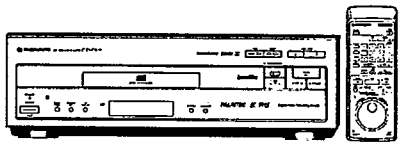
PIONEER®
The Art of Entertainment

Service Manual



ORDER NO.
RRV1546

CD CDV LD PLAYER

CLD-D925

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Type	Model	Power Requirement	Remarks
	CLD-D925		
WY	○	AC220-240V	
WV	○	AC220-240V	

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1. SAFETY INFORMATION

VARO!
AVATTAESSA JA SUOJALUKITUS OHITETTAESSA OLET ALTTIINA NÄKYMÄTTÖMÄLLE LASERSÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN.

ADVERSEL
USYNLIG LASERSTRÅLING VED ÅBNING NÅR SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION UNDGÅ UDSAETTELSE FOR STRÅLING.

VARNING!
OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD OCH SPÄRREN ÄR URKOPPLAD. BETRAKTA EJ STRÅLEN.

LASER
Kuva 1
Lasersäteilyn varoitusmerkki

WARNING!
DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.

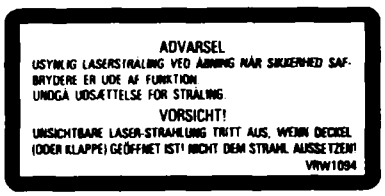
IMPORTANT
THIS PIONEER APPARATUS CONTAINS LASER OF CLASS 1.
SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

LASER DIODE CHARACTERISTICS
MAXIMUM OUTPUT POWER: 5 mw
WAVELENGTH: 780-785 nm

LASER
Picture 1
Warning sign for laser radiation

LABEL CHECK

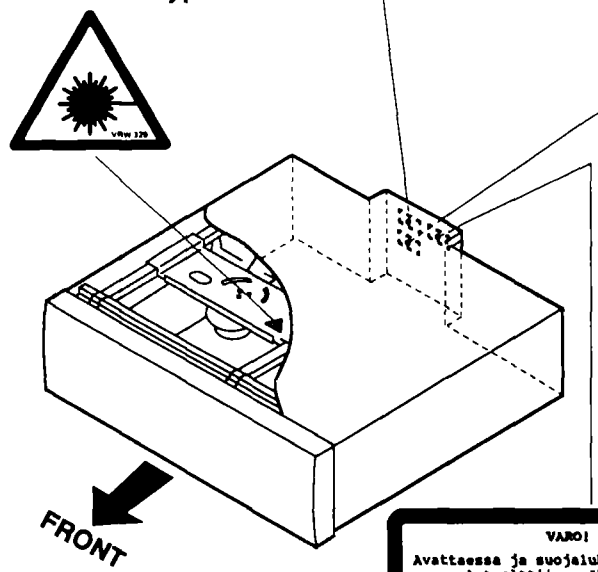
WY type


ADVARSEL
USYNLIG LASERSTRÅLING VED ÅBNING NÅR SIKKERHED SAF-
BRYDERE ER UDE AF FUNKTION
UNDGÅ UDSÆTTELSE FOR STRÅLING
VORSICHT!
UNSICHTBARE LASER-STRAHLUNG TRITT AUS, WENN DECKEL
(ODER KLAPPE) GEÖFFNET IST! NICHT DEM STRAHL AUSSETZEN!
VRW1094

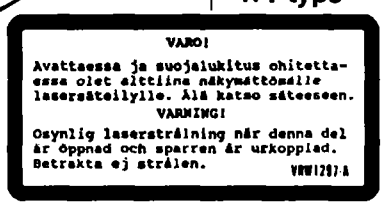
WV type

WY and WV types

WY and WV types



WY type


VARO!
Avattaessa ja suojalukitus ohitettaessa olet alttiina näkymättömälle lasersäteilylle. Älä katso säteeseen.
VARNING!
Osynlig laserstrålning när denna del är öppnad och spärren är urkopplad. Betrakta ej strålen.

Additional Laser Caution

1. The ON/OFF statuses of the side-A/B detection switch (**TURN** switch on the **TNSB** assy), slider-position detection switches (**INNER** and **OUTER** on the **PKSB** assy) and loading-status detection switches (**SW 1, 2** and **3** on the **LMSB** assy) are detected by the microprocessor (**IC101** in the **MAIN** assy). To permit the laser diode to oscillate, it is required to set the side-A/B detection switch for side A status (**TRN : OFF**) and the slider-position detection switches for the LD ACTIVE status (**INNER : OFF, OUTER : OFF**), and to set the loading-status detection switches for tilt neutral state (**SW1 : OFF, SW2 : OFF, SW3 : ON**). As long as these requirements are not satisfied, the laser diode will not oscillate. When the requirements are met in any way, the laser diode can oscillate. The laser diode oscillation will continue if pin 13 of **IC801** is shorted to **GND** or the emitter and collector of **Q834** are shorted each other (fault condition) in **MAIN** assy.
   In the test mode ＊, the laser diode oscillates when the microprocessor detects a PLAY signal, or when the PLAY key is pressed (**S106 ON** in the **FLKY** assy, with the above requirements satisfied.
2. When the cover is open, close viewing through the objective lens with the naked eye will cause exposure to a Class 1 laser beam.

＊ : Refer to pages 44 and 45.

2. PACKING, EXPLODED VIEWS AND PARTS LIST

NOTES:

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

2.1 PACKING

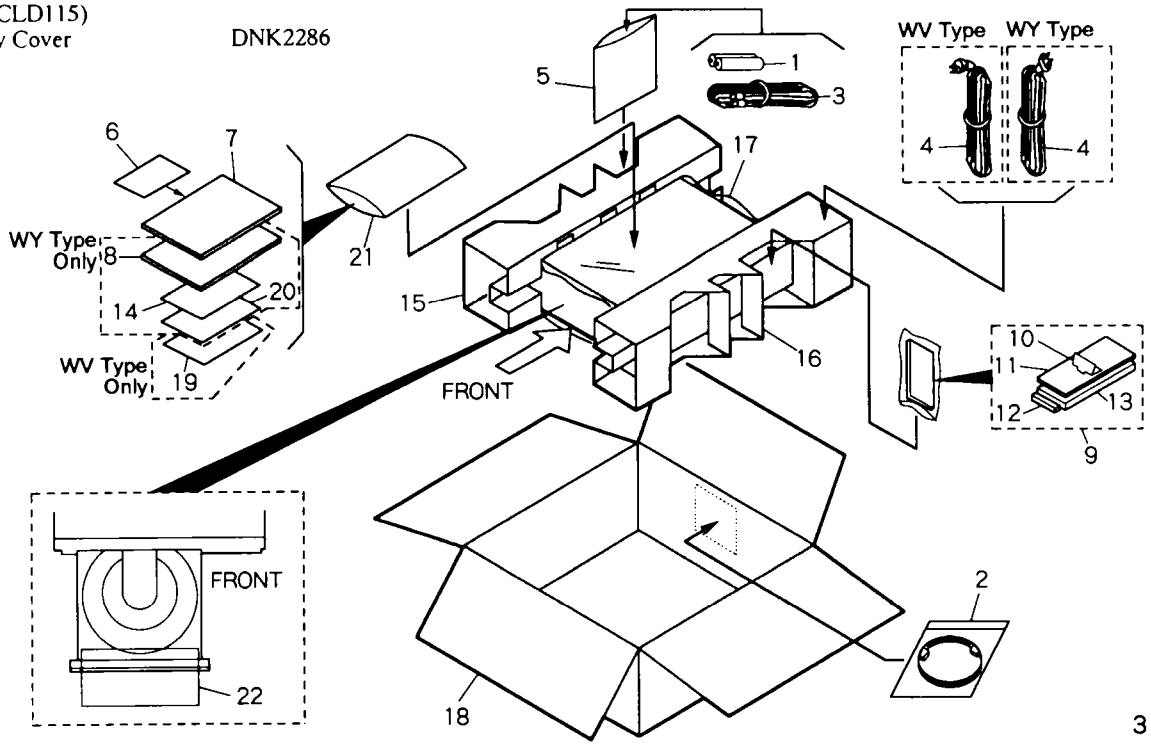
(1) CONTRAST OF CLD-D925/WY AND WV

CLD-D925/WY and WV have the same construction except for the following:

Mark	No.	Symbol & Description	Part No.		Remarks
			WY type	WV type	
⚠	4	Power Cord	ADG1154	ADG1156	
	8	Operating Instructions (Dutch/Swedish/Spanish/Portuguese)	VRF1037	Not used	
NSP	14	Caution	VRR1009	Not used	
	19	Caution (UC)	Not used	VRR1020	
NSP	20	Caution (EW)	VRM1027	Not used	

(2) PARTS LIST FOR CLD-D925/WY

Mark	No.	Description	Part No.
NSP	1	Dry Cell Batteries (R03, AAA)	VEM-022
	2	Euroconnector Cable	VDE1031
	3	Audio Cord	VDE1033
⚠	4	Power Cord	ADG1154
	5	Polyethylene Bag (0.03*230*340)	Z21-038
NSP	6	Warranty Card	ARW-088
	7	Operating Instructions (English/French/German/Italian)	VRE1047
	8	Operating Instructions (Dutch/Swedish/Spanish/Portuguese)	VRF1037
	9	Remote Control Unit (CU-CLD115)	VXX2242
	10	Battery Cover	DNK2286
	11	Case (Under)	VNK2062
	12	Filter	VNK2063
	13	Case (Upper)	VNK3134
NSP	14	Caution	VRR1009
	15	Protector L	VHB1054
	16	Protector R	VHB1055
	17	Mirror Mat	VHL1012
	18	Packing Case	VHG1581
	19	• • • • •	
NSP	20	Caution (EW)	VRM1027
NSP	21	Polyethylene Bag	VHL-014
	22	Mirror Mat Sheet	VHL1039



2.2 EXTERIOR AND DISC TRAY SECTION

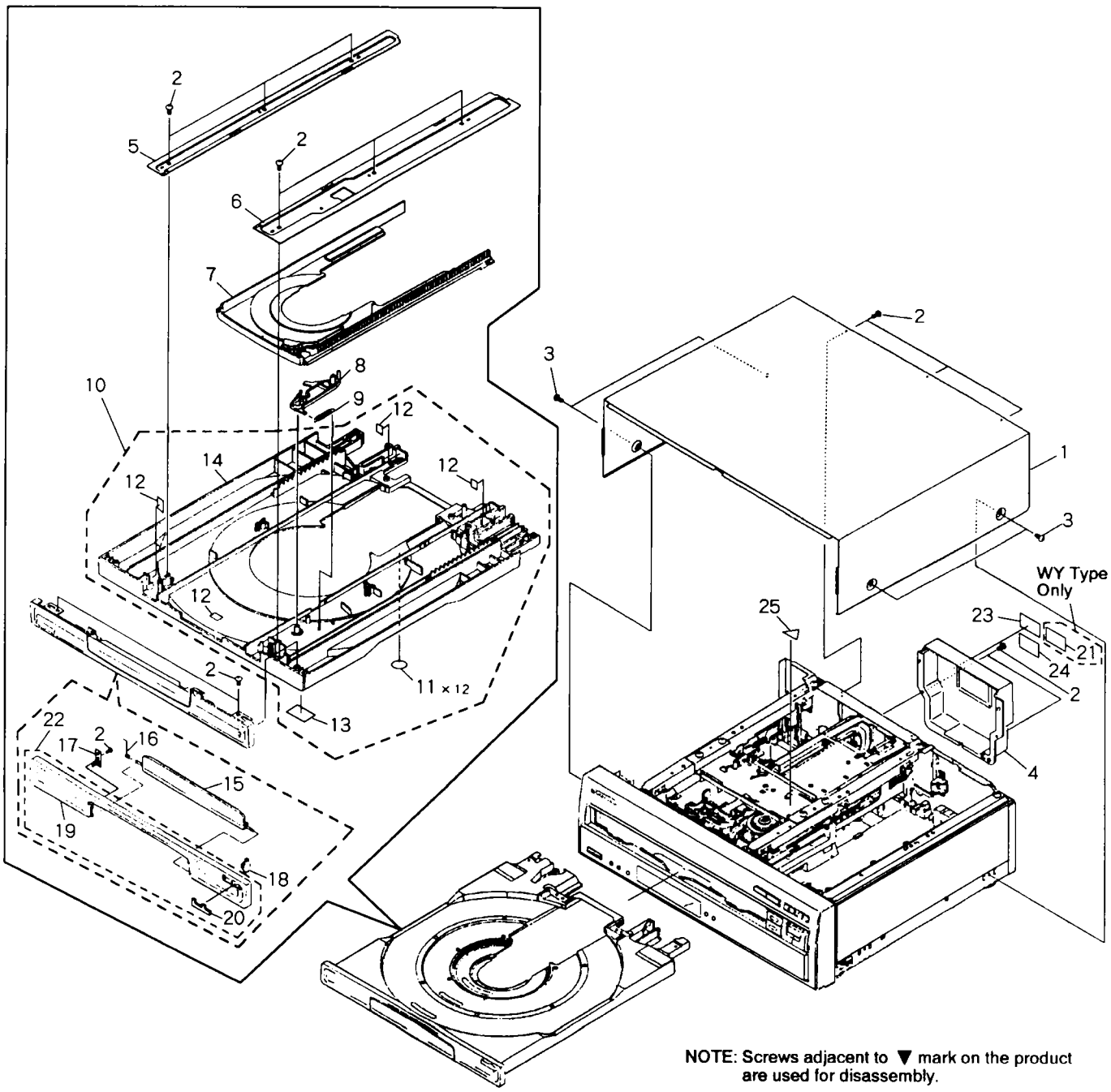
(1) CONTRAST OF CLD-D925/WY AND WV

CLD-D925/WY and WV have the same construction except for the following:

Mark	No.	Symbol & Description	Part No.		Remarks
			WY type	WV type	
NSP	21	Caution Label HE	VRW1297	Not used	
	23	Caution Label	VRW1094	PRW1018	

(2) PARTS LIST FOR CLD-D925/WY

Mark	No.	Description	Part No.
	1	Bonnet S	VXX2252
	2	Screw	BBZ30P080FMC
	3	Screw	BCZ40P060FZK
	4	Rear Cover	VNK3767
	5	Guide Plate (R)	VNE1939
	6	Guide Plate (L)	VNE1938
	7	CD Tray	VNK3007
	8	Lock Plate	VNL1703
	9	Lock Plate Spring	VBH1188
	10	Tray Assy-S	VXX2307
	11	Cushion	VEC1682
	12	Damp Cushion	VEC1683
NSP	13	Label	VRW1289
	14	LD Tray Assy	VXA2173
	15	CD Door Assy	VXA2275
	16	Door Spring	VBH1248
	17	Door Holder	VNL1704
	18	Damper Assy	VXA1999
	19	Tray Panel	VNK3624
	20	Name Plate	VAM1029
NSP	21	Caution Label HE	VRW1297
	22	Tray Panel Assy-S	VXX2409
	23	Caution Label	VRW1094
NSP	24	Caution Label (F)	VRW-328
	25	Caution Label (G)	VRW-329

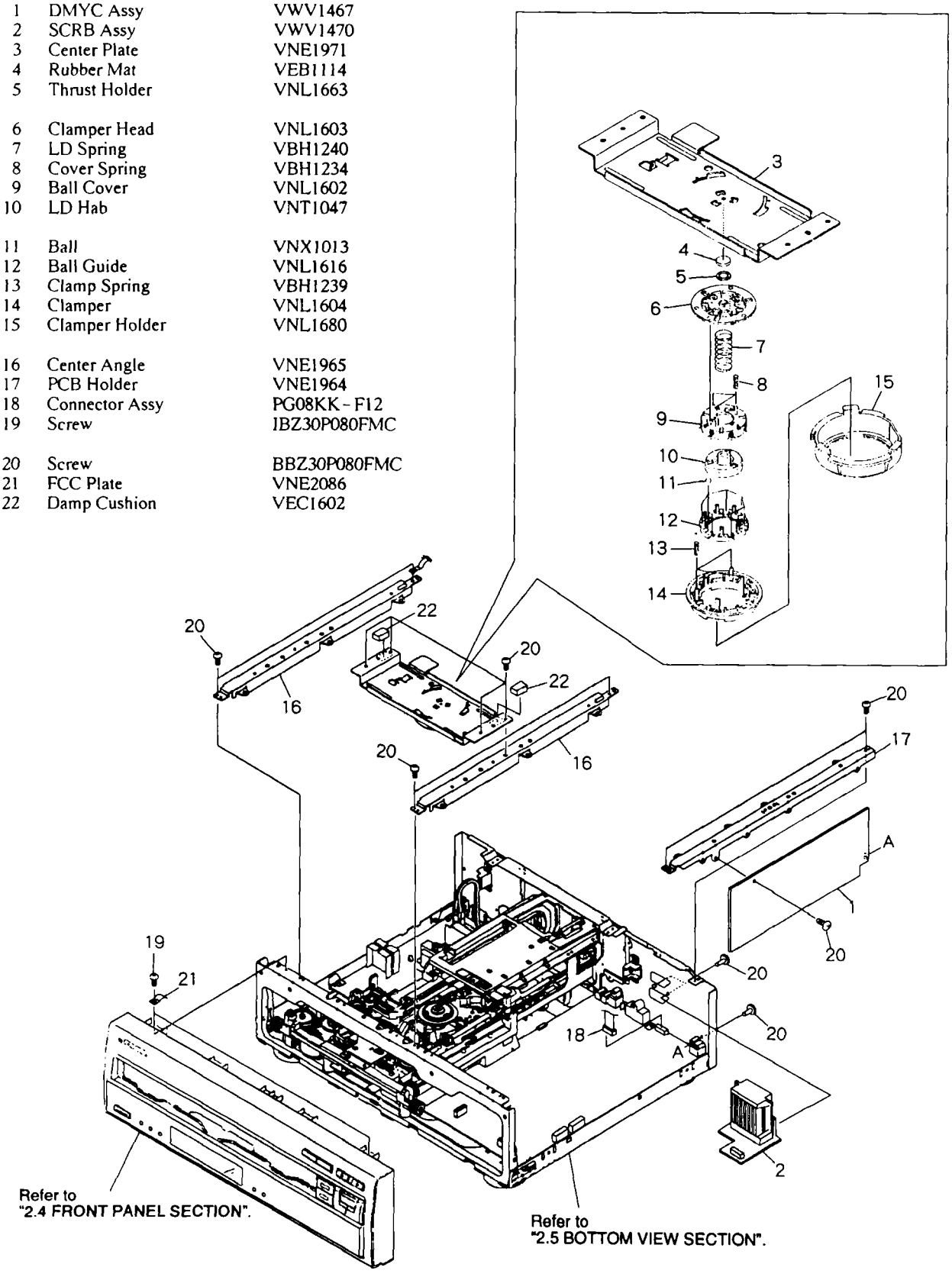


NOTE: Screws adjacent to ▼ mark on the product are used for disassembly.

2.3 TOP VIEW SECTION

Parts List

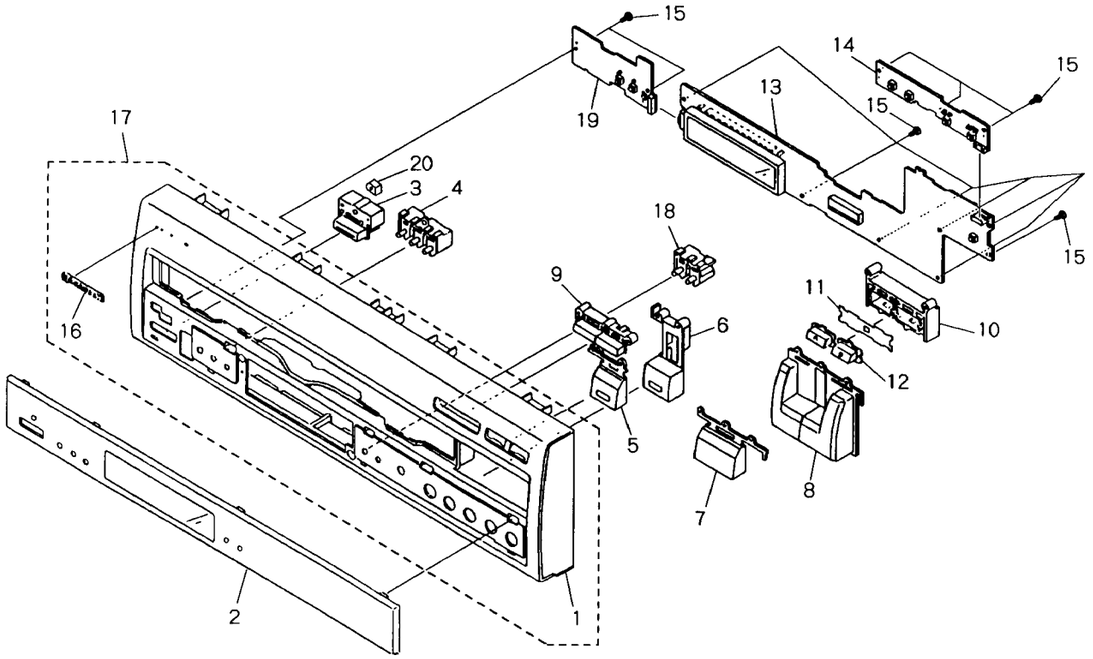
Mark	No.	Description	Part No.
	1	DMYC Assy	VWV1467
	2	SCRB Assy	VWV1470
	3	Center Plate	VNE1971
	4	Rubber Mat	VEB1114
	5	Thrust Holder	VNL1663
	6	Clamper Head	VNL1603
	7	LD Spring	VBH1240
	8	Cover Spring	VBH1234
	9	Ball Cover	VNL1602
	10	LD Hab	VNT1047
	11	Ball	VNX1013
	12	Ball Guide	VNL1616
	13	Clamp Spring	VBH1239
	14	Clamper	VNL1604
	15	Clamper Holder	VNL1680
	16	Center Angle	VNE1965
NSP	17	PCB Holder	VNE1964
	18	Connector Assy	PG08KK-F12
	19	Screw	IBZ30P080FMC
	20	Screw	BBZ30P080FMC
	21	FCC Plate	VNE2086
NSP	22	Damp Cushion	VEC1602



2.4 FRONT PANEL SECTION

Parts List

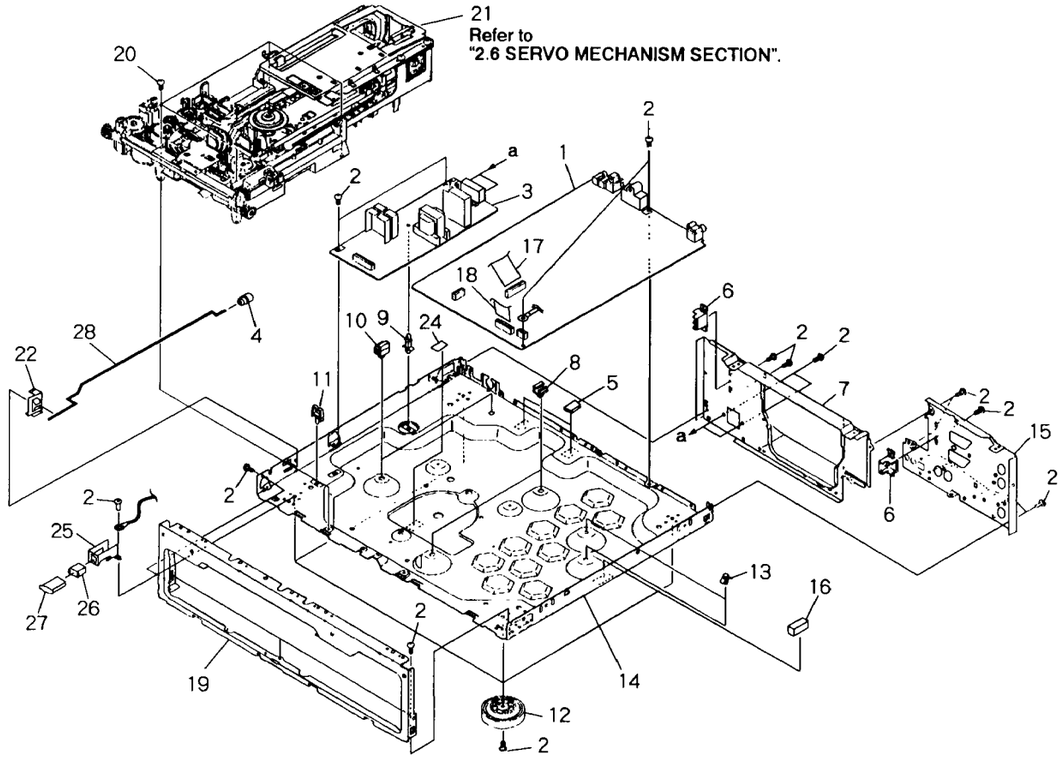
Mark	No.	Description	Part No.
NSP	1	Front Panel	VNK3765
	2	FL Panel	VNK3766
	3	Power Button	VNK3705
	4	L Key B	VNK3008
	5	LD Key Assy	VXA2276
	6	CD Key Assy	VXA2277
	7	Play Key	VNK3720
	8	Key A	VNK3719
	9	Skip Key	VNK3630
	10	LED Holder	VNK3467
	11	Sheet	VEC1849
	12	Disc Side Key	VNK3468
	13	FLKY Assy	VWG1743
NSP	14	KEYB Assy	VWG1728
	15	Screw	BBZ30P080FMC
	16	Name Plate	PAM1704
	17	Front Panel Assy - S	VXX2427
	18	Key K	VNK2998
	19	PWSB Assy	VWG1744
	20	LED Lens	PNW2019



2.5 BOTTOM VIEW SECTION

Parts List

Mark	No.	Description	Part No.
NSP	1	MAIN Assy	VWS1240
	2	Screw	BBZ30P080FMC
⚠	3	SYPS Assy	VWR1275
	4	Joint Cap	DEB1057
NSP	5	Rubber Spacer	VEB1252
	6	Tray Stopper	VNL1657
	7	Rear Panel (R)	VNA1713
NSP	8	P Plate Holder	PNY - 405
NSP	9	PC Support	VEC - 269
NSP	10	PCB Hinge	VEC1174
NSP	11	Wire Clip (H)	VEC1181
	12	Insulator	PNW1912
	13	Card Spacer A	VEC1708
NSP	14	Chassis	VNA1564
	15	Rear Panel (L)	VNA1712
	16	Spacer	REB1171
	17	Flexible Cable (21P)	VDA1465
	18	Flexible Cable (16P)	VDA1488
NSP	19	Panel Holder	VNA1507
	20	Screw	BBZ30P100FMC
NSP	21	Mechanism Assy	VWT1131
	22	Shaft Holder	DNK2414
	23	• • • • •	
NSP	24	Spacer	VEC - 244
NSP	25	Bush Holder	VNE2063
	26	PSW Bush	DNK1326
	27	PSW Cap	DNK1325
NSP	28	PSW Joint	VLL1487

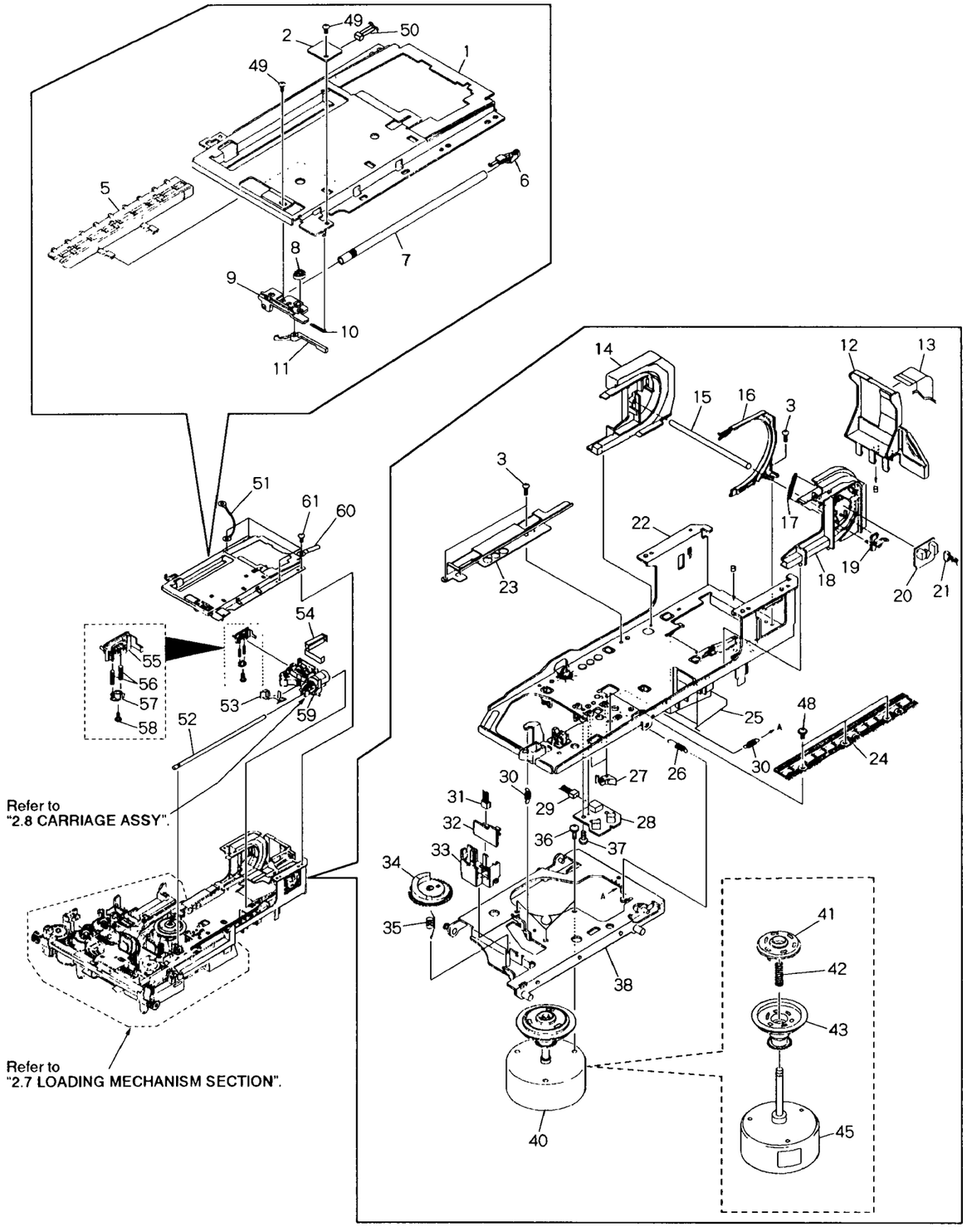


2.6 SERVO MECHANISM SECTION

Parts List

Mark	No.	Description	Part No.
	1	Tilt Base (upper)	VNE1969
NSP	2	BISB Assy	VWG1558
	3	Screw	BBZ30P060FMC
	4	• • • • •	
	5	Rack (Upper)	VNL1679
	6	Shaft Stay	VNL1671
	7	Carriage Shaft (upper)	VLL1478
	8	B Cam	VNL1673
	9	Shaft Support	VNL1672
	10	Support Spring	VBH1265
	11	SW Lever (B)	VNL1678
	12	Large hill	VNL1682
	13	Flexible Cable (23P)	VDA1528
	14	Turn Guide	VNL1701
	15	FFC Style Shaft	VLL1474
	16	Guide	VNL1674
	17	Lever Spring	VBH1266
	18	Turn Gear	VNL1702
	19	SW Lever (T)	VNL1695
NSP	20	TNSB Assy	VWG1557
	21	Housing Assy (3P, Black)	VKP2059
	22	Tilt Base (Under)	VNL1670
	23	TAN Guide	VNE1973
	24	CA Rack	VNL1647
	25	FFC Style Spring	VBH1270
	26	Thrust Spring	VBH1245
	27	CA - SW Lever	VNL1644
NSP	28	PKSB Assy	VWG1555
	29	Housing Assy (3P, Blue)	VKP2045
	30	Tilt Spring	VBH1263

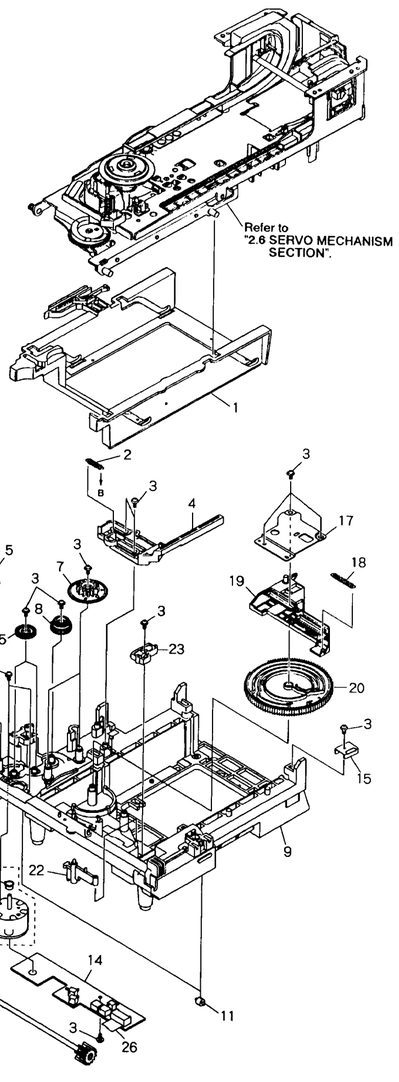
Mark	No.	Description	Part No.
	31	Housing Assy (3P, Yellow)	VKP2046
NSP	32	FG Assy	VWG1556
	33	FG Base	VNL1645
	34	Tilt Cam	VNL1643
	35	Tilt Cam Spring	VBH1243
	36	Screw	PMA30P050FMC
	37	Screw	IBZ26P120FMC
	38	Motor Base	VNE1941
	39	• • • • •	
	40	Spindle Motor Assy	VXA2271
	41	PRC Hub	VNL1684
	42	Centering Spring	VBH1269
NSP	43	R Turn Table Assy	VXA2225
	44	• • • • •	
NSP	45	Spindle Motor	VXM1057
	46	• • • • •	
	47	• • • • •	
	48	Screw	IBZ26P060FMC
	49	Screw	BPZ20P040FZK
	50	Housing Assy (2P, Red)	VKP2060
NSP	51	Earth Lead Unit	DE007VF0
	52	Carriage Shaft (Under)	VLL1493
	53	Body Guard	VNL1681
	54	FFC Holder	VNL1706
	55	CA Guide	VNL1668
	56	TAN Spring (B)	VBH1264
	57	TAN Lever (B)	VNL1669
	58	Screw	PMZ20P060FZK
⚠	59	Carriage Assy	VWT1110
NSP	60	Cord Binder	ZCB - 069Z
	61	Screw	BBZ30P080FMC



2.7 LOADING MECHANISM SECTION

Parts List

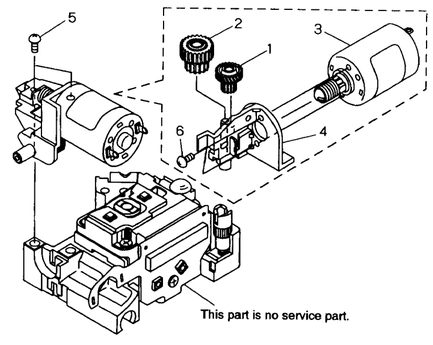
Mark	No.	Description	Part No.
	1	Clamp Cam	VNL1633
	2	CDP Spring	VBH1191
	3	Screw	Z39-019
	4	CD Plate	VNL1685
	5	Rubber Belt	VEB1184
	6	Gear Pulley	VNL1662
	7	Twin Gear	VNL1626
	8	Center Gear	VNL1660
	9	Mechanism Base	VNK3239
	10	Screw	BMZ26P040FMC
	11	Roller	VNL1042
NSP	12	Motor Pulley	VNL1630
	13	Synchro Gear Assy	VXA2105
NSP	14	LMSB Assy	VWG1612
	15	Cam Holder	VNE2032
NSP	16	Carriage Motor	VXM1033
	17	Shaft Holder	VNE1942
	18	CAS Spring	VBH1190
	19	Cam Plate	VNL1631
	20	Cam Gear	VNL1625
	21	Loading Motor Assy	VXX2045
	22	MB-SW Lever	VNL1664
	23	Slider (R)	VNL1666
	24	Slider (L)	VNL1665
	25	Double Gear	VNL1661
	26	Flexible Cable (12P)	VDA1485



2.8 CARRIAGE ASSY

Parts List

Mark	No.	Description	Part No.
	1	CA Gear (A)	VNL1638
	2	CA Gear (B)	VNL1639
	3	Slider Motor Assy	VXX2082
	4	M Holder	VNL1700
	5	Screw	PBZ20P060FMC
	6	Screw	PMZ20P030FMC



3. SCHEMATIC AND PCB CONNECTION DIAGRAMS

NOTE FOR SCHEMATIC DIAGRAMS (Type 4A)

1. When ordering service parts, be sure to refer to "PARTS LIST of EXPLODED VIEWS" or "PCB PARTS LIST".

2. Since these are basic circuits, some parts of them or the values of some components may be changed for improvement.

3. RESISTORS :
Unit : k : kΩ, M : MΩ, or Ω unless otherwise noted.
Rated power : 1/4W, 1/6W, 1/8W, 1/10W unless otherwise noted.
Tolerance : (F) : ±1%, (G) : ±2%, (K) : ±10%, (M) : ±20% or ±5% unless otherwise noted.

4. CAPACITORS :
Unit : p : pF or μF unless otherwise noted.
Ratings : capacitor (μF) / voltage (V) unless otherwise noted.
Rated voltage : 50V except for electrolytic capacitors.

5. COILS :
Unit : m : mH or μH unless otherwise noted.

6. VOLTAGE AND CURRENT :
or ← V :
DC voltage (V) in PLAY mode unless otherwise noted.
⇦mA or ← mA :
DC current in PLAY mode unless otherwise noted
Value in ( ) is DC current in STOP mode

7. OTHERS :
- ⊘ or ◉ : Adjusting point.
- ◀ : Measurement point
- The ⚠ mark found on some component parts indicates the importance of the safety factor of the parts. Therefore, when replacing, be sure to use parts of identical designation.

8. SCH – □ ON THE SCHEMATIC DIAGRAM :
- SCH-□ indicates the drawing number of the schematic diagram. (SCH stands for schematic diagram)

9. SWITCHES (Underline indicates switch position) .

LMSB ASSY
S101 : SW1
S102 : SW2
S103 : SW3

PKSB ASSY
S104 : INNER
S105 : OUTER

BISB ASSY
S112 : B INSIDE

TNSB ASSY
S111 : TURN

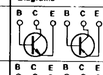
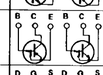
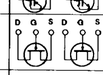
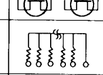
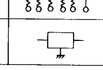
FLKY ASSY
S101 : SYSTEM
S102 : LANGUAGE
S103 : OPEN/CLOSE (CD ⏏)
S104 : OPEN/CLOSE (LD ⏏)
S105 : STOP(■)
S106 : PLAY(▶)
S107 : PAUSE(❚❚)

KEYB ASSY
S201 : B] DISC SIDE
S202 : A]
S203 : ▶▶ ▶▶| (FWD)
S204 : |◀◀ ◀◀ (REV)

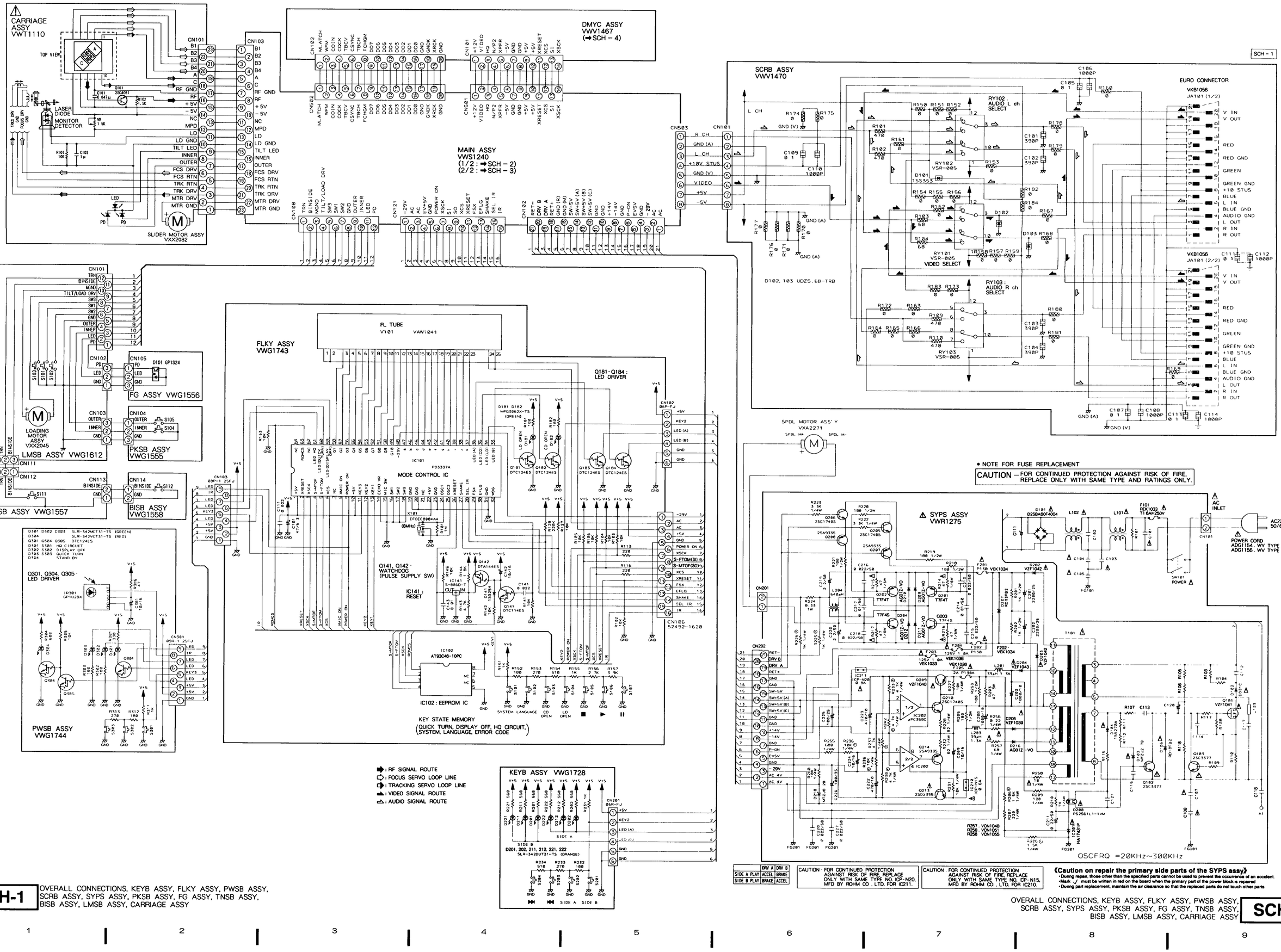
PWSB ASSY
S301 : HQ CIRCUIT
S302 : DISPLAY OFF
S303 : QUICK TURN

SYPS ASSY
SW101 : POWER ON/OFF

NOTE FOR PCB DIAGRAMS:
1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

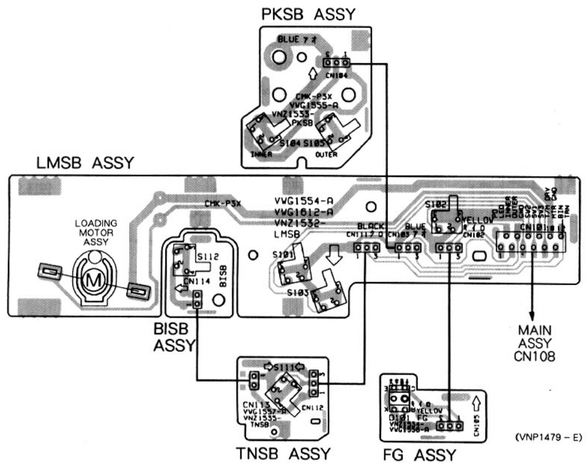
Symbol in PCB Diagrams	Symbol in Schematic Diagrams	Part Name
		Transistor
		Transistor with resistor
		Field effect transistor
		Resistor array
		3-terminal regulator

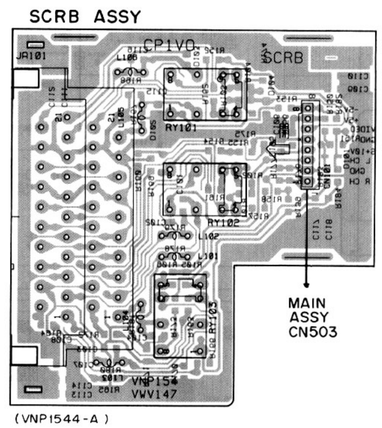
3.1 OVERALL CONNECTIONS, KEYB, FLKY, PWSB, SCRB, SYPS, PKSB, FG, TNSB, BISB, LMSB AND CARRIAGE ASSEMBLIES

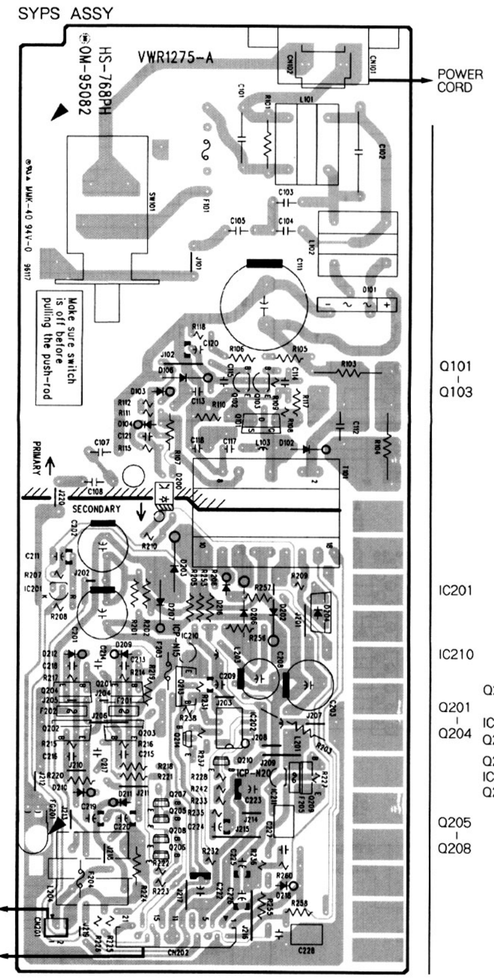

CARRIAGE ASSY VWT1110
TOP VIEW
LASER DIODE
MONITOR DETECTOR
SLIDER MOTOR ASSY VXX2082
DMYC ASSY VWV1467 (➡SCH-4)
MAIN ASSY VWS1240 (1/2:➡SCH-2) (2/2:➡SCH-3)
SCRB ASSY VWV1470
RY102: AUDIO L ch SELECT
RY101 VSR-005 VIDEO SELECT
RY103: AUDIO R ch SELECT
EURO CONNECTOR VKB1056 JA101 (1/2)
VKB1056 JA101 (2/2)
D102, 103 UDZ5.6B-TRB
SPDL MOTOR ASS'Y VXA2271
FLKY ASSY VWG1743
FL TUBE V101 VAW1041
MODE CONTROL IC PD3337A
Q181-Q184: LED DRIVER
Q141, Q142: WATCHDOG (PULSE SUPPLY SW)
IC141: RESET
IC102: EEPROM IC
KEY STATE MEMORY (QUICK TURN, DISPLAY OFF, HQ CIRCUIT, SYSTEM, LANGUAGE, ERROR CODE)
LMSB ASSY VWG1612
FG ASSY VWG1556
PKSB ASSY VWG1555
TNSB ASSY VWG1557
BISB ASSY VWG1558
PWSB ASSY VWG1744
KEYB ASSY VWG1728
SYPS ASSY VWR1275
AC INLET
POWER CORD ADG1154: WY TYPE ADG1156: WY TYPE
AC220-240V 50/60Hz
OSCFRQ =20KHz~300KHz
• NOTE FOR FUSE REPLACEMENT
CAUTION – FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE AND RATINGS ONLY.
➡: RF SIGNAL ROUTE
⇨: FOCUS SERVO LOOP LINE
➡: TRACKING SERVO LOOP LINE
▲: VIDEO SIGNAL ROUTE
△: AUDIO SIGNAL ROUTE
CAUTION · FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE NO. ICP-N20, MFD BY ROHM CO., LTD. FOR IC211.
CAUTION . FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE NO. ICP-N15, MFD BY ROHM CO., LTD. FOR IC210.
(Caution on repair the primary side parts of the SYPS assy)
• During repair, those other than the specified parts cannot be used to prevent the occurrence of an accident.
• Mark √ must be written in red on the board when the primary part of the power block is repaired
• During part replacement, maintain the air clearance so that the replaced parts do not touch other parts

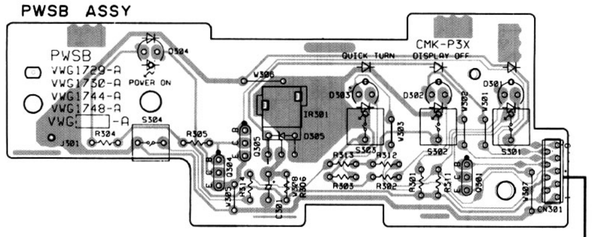
SCH-1 OVERALL CONNECTIONS, KEYB ASSY, FLKY ASSY, PWSB ASSY, SCRB ASSY, SYPS ASSY, PKSB ASSY, FG ASSY, TNSB ASSY, BISB ASSY, LMSB ASSY, CARRIAGE ASSY

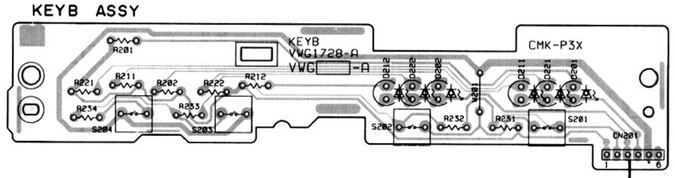
PCB – 1



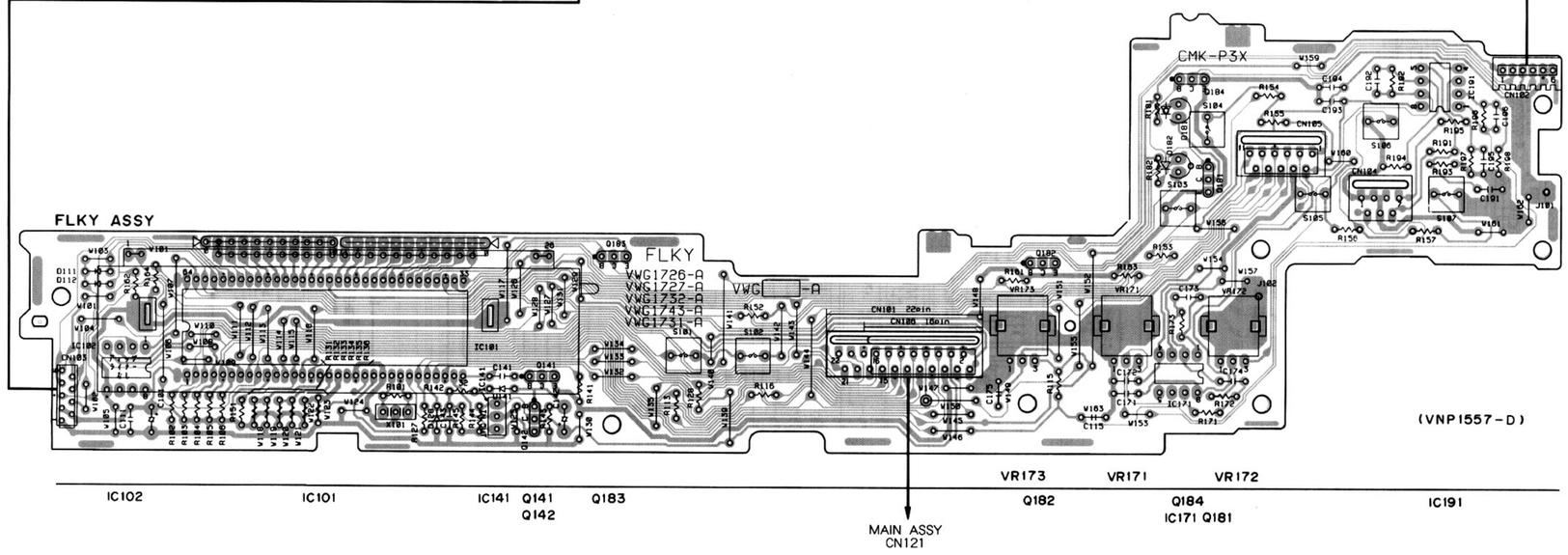




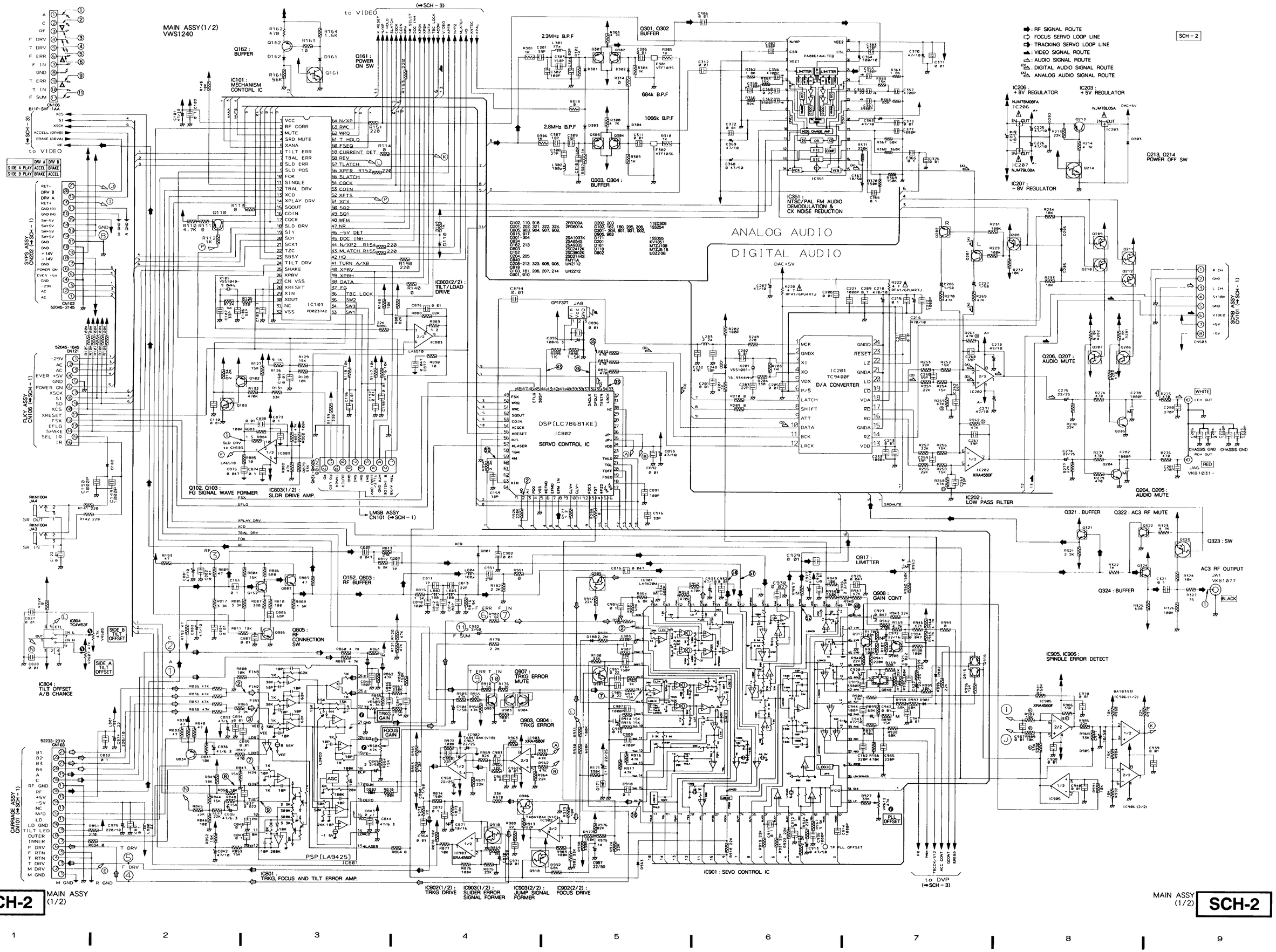




- This diagram is viewed from the mounted parts side.
- The parts mounted on this PCB include all necessary parts for several destinations.
  For further information for respective destinations, be sure to check with the schematic diagram.



3.2 MAIN ASSY (1/2)



WAVEFORMS AND VOLTAGE

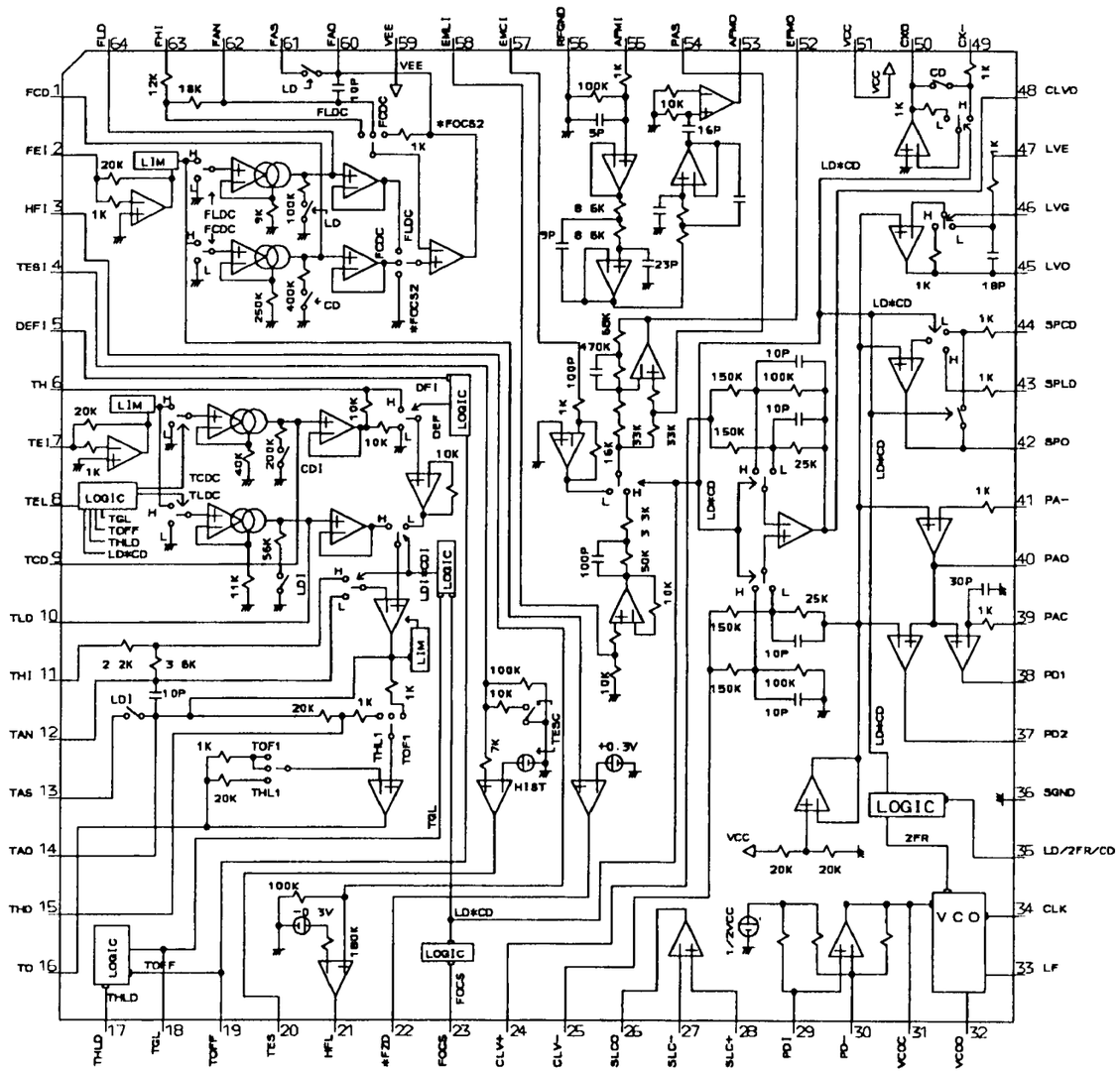
MAIN ASSY (1/2)

Note : (No) in the table correspond to the pin number.

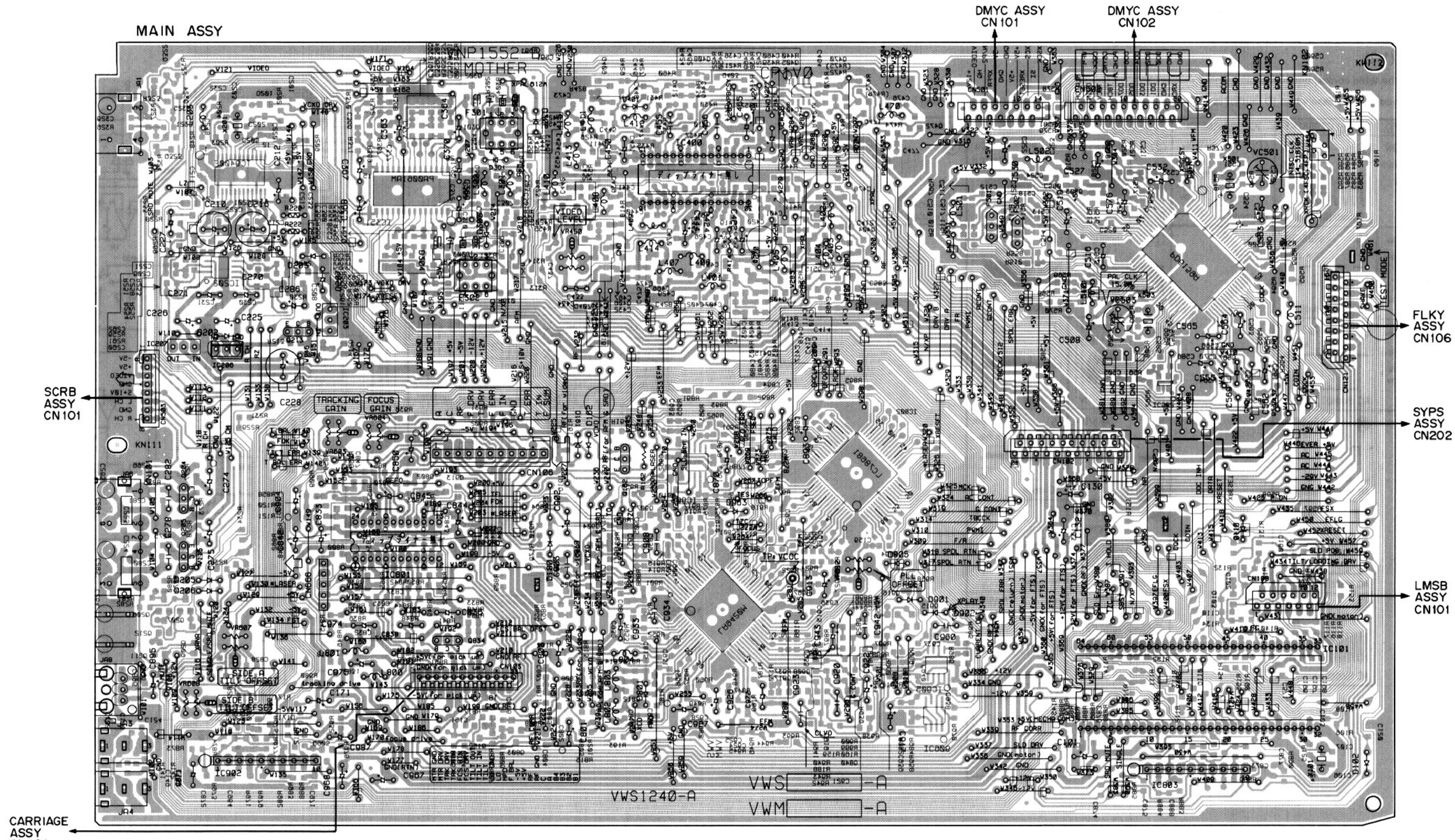
Measurement condition : In case when (D. audio) is written, at time when disc that has digital audio recording is played.

IC801(LA9425)	IC802(LC78681KE)	IC803(LA6510)	IC901(LA9420M)	CN106	Video output pin
②, ③ 1mS/Div 16mVp-p AC mode	② 0.1μS/Div 4.3Vp-p AC mode(D audio)	① 2mS/Div. 1.8Vp-p DC mode	② 0.2mS/Div 74mVp-p DC mode	①, ② 5mS/Div 65mVp-p DC mode	① approx. 1Vp-p (75Ω termination) V 20mV/Div H 10mS/Div
⑦, ⑧ 1mS/Div 67mVp-p 0V DC mode	㉝ 10μS/Div 4.2Vp-p AC mode(D audio)		⑦ 0.2mS/Div 74mVp-p 0V DC mode	③ 0.5mS/Div 300mVp-p AC mode	
⑨ 5mS/Div 0.1Vp-p 0V DC mode	㉟ 0.2μS/Div 4.4Vp-p AC mode(D audio)		⑯ 0.2mS/Div. 0.61Vp-p DC mode 0V	④ 5mS/Div 15Vp-p DC mode	
	㊱ 0.2μS/Div 4.5Vp-p AC mode(D audio)		㊽ 50μS/Div 6.2Vp-p DC mode	⑤ 5mS/Div. 5.8Vp-p DC mode	
	㊸ 0.1μS/Div 4.5Vp-p AC mode(D audio)		㊷ 0.2μS/Div. 2.1Vp-p AC mode	⑥ 5mS/Div 3.5Vp-p DC mode	
	㊾ 0.1μS/Div 2Vp-p AC mode(D audio)		㊼ 1mS/Div 0.53Vp-p DC mode 0V	⑨ 5mS/Div 1.25Vp-p DC mode	
			㊽ 0.2mS/Div 0.32Vp-p 0V DC mode	⑪ 10mS/Div 1.7Vp-p DC mode	

• The inside block diagram of IC901 (LA9420M)



PCB-2



VR608 VR607 VR603 VR604 VR450 VR612 VC503 VC501

IC207 IC206 Q213 IC203 IC801 Q834 Q162 IC400 IC803 IC101

Q204 Q205 IC902

- This diagram is viewed from the mounted parts side.
- The parts mounted on this PCB include all necessary parts for several destinations.
  For further information for respective destinations, be sure to check with the schematic diagram.

WAVEFORMS AND VOLTAGE

MAIN ASSY (2/2)

Note : (No.) in the table correspond to the pin number.

IC400 (LA7133)

(10) 1.52Vp-p, 0.55V — V : 20mV/Div, H : 10mS/Div

(8) (TOP) 2.4V, (BOTTOM) 1.85V, 0.55V — V : 20mV/Div, H : 10mS/Div

(12) 1Vp-p, 1.65V — V 20mV/Div, H 10mS/Div

(14) 1Vp-p — V 20mV/Div, H 10mS/Div

(23) (No noise)

(25) (with limiter noise) — V 20mV/Div, H 10mS/Div, approx. 330mVp-p

(27) approx. 1Vp-p — 0.5mS/Div

IC500 (PD6159A)

(4) XTBCV (at PAL) V : 0.5V/Div H : 20μS/Div — High (5V) at NTSC, VIDEO OUTPUT WAVEFORM, 5V, 0V (4), 20 or 333H, 21 or 334H

(37) ADIN (at PAL) V : 0.5V/Div H : 10μS/Div — 0V

(58) DC02 (60) DC05 (61) DC07 V : 0.5V/Div H : 50nS/Div — 0V (58), 0V (60), 0V (61)

(37) ADIN (at PAL) (45) PBCLP (PILOT BURST CLAMP PULSE) V : 0.5V/Div H : 10μS/Div — Low (0V) at NTSC, 5V, 0V, (37), (45)

(64) AD CKP (at PAL) (15.0MHz) (65) AD CKIN (at NTSC) (14.31818MHz) V : 50mV/Div H : 20nS/Div — VDC = 2.36V, 0V (AC)

(22) RCK/XRCK (at NTSC BLUE BACK and PLAY) 4fsc = 14.31818MHz; RCK/XRCK (at PAL BLUE BACK) 4fsc = 17.73447SMHz V 0.5V/Div H 50nS/Div — 0V

(41) XPB CSY (X PLAY BACK COMPOSITE SYNC) V : 0.5V/Div H : 10μS/Div — 0V

(70) DC01 (at PAL) (3.75MHz) DC01 (at NTSC) (3.58MHz) V : 50mV/Div H : 0.1μS/Div — VDC = 2.4V, 0V (AC)

(22) RCK/XRCK (at PAL DISC PLAY) 4fsp = 15.0MHz V : 0.5V/Div H : 50nS/Div — 0V

(44) RF (at PLAY) V : 0.1V/Div H : 5mS/Div — 2.2VDC at PLAY, 2.4VDC at STOP, 0V

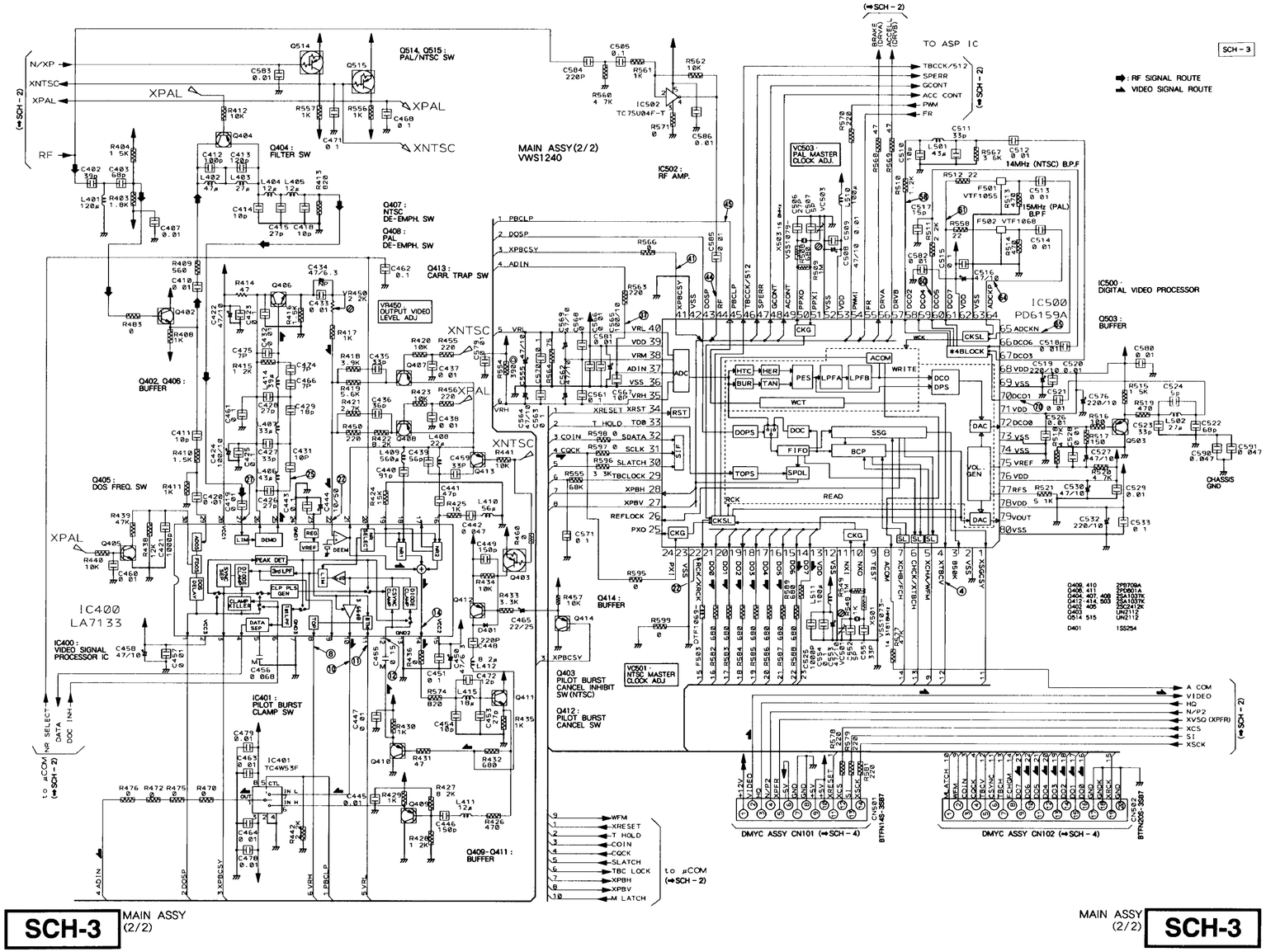
Note : Values indicate the voltage in the play mode. play mode.

IC400 (LA7133)

Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	4.25	16	2
2	5	17	2.05
3	0.1	18	2
4	0.25	19	0.8
5	1.9	20	2.5
6	2.5	21	2.75
7	0	22	2.75
8	2.4	23	4.25
9	1.05	24	0
10	0.65	25	3.4
11	0.55	26	5
12	1.7	27	3.2
13	0	28	5
14	2.75	29	3.2
15	5	30	1.05

IC500 (PD6159A)

Pin	VDC (V)
35	2.40
38	1.475
40	0.55
75	2.5
77	2.5



SCH-3 MAIN ASSY (2/2)

MAIN ASSY (2/2) SCH-3

DMYC ASSY VWV1467

XRGB	NTSC	PAL	QUASI-PAL
NORMAL PLAY	H	H	L
TRICK PLAY	H	L	L

IC101 : MEMORY CONTROLLER IC

IC102 : FIELD MEMORY

IC201 : DIGITAL 3LINE Y/C

IC301 : D/A CONVERTER

IC401 : 4fsc CLOCK GENERATOR

IC601 : PHASE COMPARATOR

IC602 : SAMPLE/HOLD

IC603 : VCXO

IC604 : CLOCK OSCILLATOR

IC605 : 1/4 CYCLE DIVIDE

IC606 : CLOCK AMP.

IC607 : SAMPLE/HOLD PULSE GENERATOR

IC701 : RGB DECODER

IC702 : RGB ENCORDER

IC831 : Y SIGNAL NOISE REDUCTION

IC991 : +5V REGULATOR

Q201 : V-DRIVE

Q202 : N/P INVERTER SW

Q232, Q241 : BUFFER

Q254, Q251 : DC VOLTAGE SHIFT

Q263, Q266 : SYNC TIP CLAMP

Q102 : CLOCK SHUT OFF SW

Q103 : N/P INV. SW

Q301, Q302 BUFFER

Q351 : PHASE COMPENSATE

Q801 : H-DRIVE

Q811, Q812 : SYNC TIP CLAMP

Q882 : NOTCH ON/OFF SW

Q808 NOTCH ON/OFF SW

Q851, Q852 : 75Ω DRIVE

Q805 : PHASE COMPENSATE

Q991, Q992 : POWER ON SW

Q701 - Q713 : NTSC/PAL SW

: VIDEO SIGNAL ROUTE
(Y) : Y SIGNAL ROUTE
(C) : C SIGNAL ROUTE
(R) : R SIGNAL ROUTE
(G) : G SIGNAL ROUTE
(B) : B SIGNAL ROUTE

SCH-4

S-OUTPUT TERMINAL

VIDEO OUTPUT (YELLOW)

DL 701 : 1H DELAY LINE (for PAL)

IC703(1/3, 3/3) : C LEVEL ADJUST VR, SUB CARRIER FREQUENCY ADJUST VR SELECT SW (NTSC/PAL)

IC703(2/3) CRYSTAL OSCILLATOR SELECT SW (NTSC/PAL)

Q201, 251, 253, 254, 264	2PB709A	Q991	2SB1237X	D991	11EQS06
Q351, 603-606, 806, 831, 834	2PB709A	Q103, 602, 701, 711, 804	DTA124EK	D992	1SR35-100AVL
Q843, 853, 864, 881, 883-887, 891	2PB709A	Q805, 832, 893	DTA124EK	D701, D702	1SS254
Q231, 232, 241, 252, 261	2PD601A	Q102, 202, 702, 703, 712	DTC124EK	D602, D711	DAP202K
Q263, 265, 266, 281-283, 301	2PD601A	Q713, 807, 813, 894, 992	DTC124EK	D601	SVC201SPA
Q302, 401, 601, 705, 801-803, 806	2PD601A				
Q808, 811, 812, 821, 822, 833, 841	2PD601A				
Q842, 851, 852, 861-863, 882, 892	2PD601A				

WAVEFORMS AND VOLTAGE

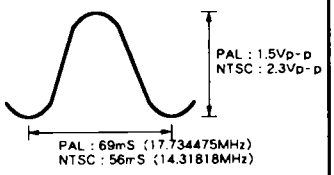
DMYC ASSY

Note : (No.) in the table correspond to the pin number.

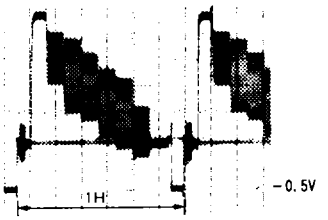
Values indicate the waveforms and voltages in the play mode.

IC201 (CXD2024AQ)

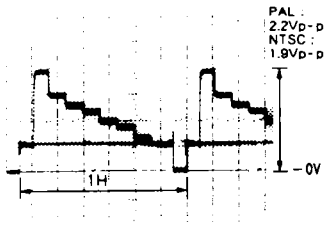
(11) OCLK



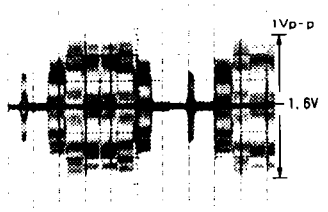
(25) AD IN (PAL)
V : 20mV/Div H : 10 µS/Div



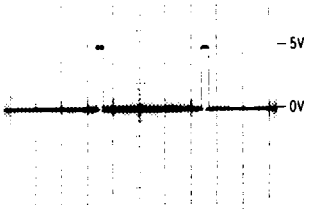
(31) AYO (at PAL)
V : 50mV/Div H : 10 µS/Div
(PAL, NTSC)



(39) ACO (at PAL)
V : 20mV/Div H : 10 µS/Div
(PAL, NTSC)

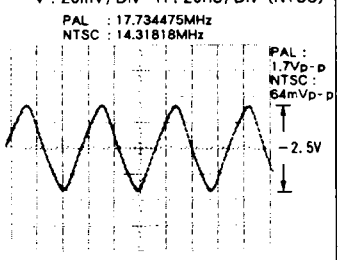


(71) TST (PAL)
V : 0.2V/Div H : 5mS/Div (PAL)

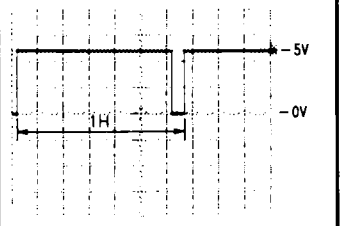


IC211 (MB90075PF-003)

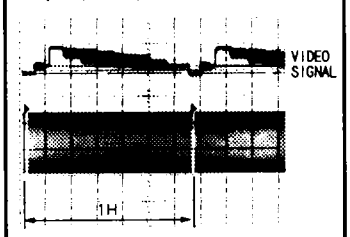
(8) EXS (at PAL)
V : 50mV/Div H : 20nS/Div (PAL)
V : 20mV/Div H : 20nS/Div (NTSC)



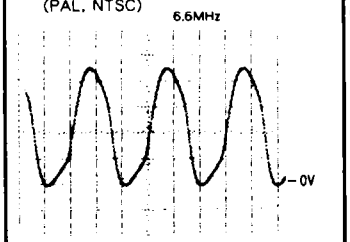
(12) EXHSYNC (at PAL)
V : 0.2V/Div H : 10 µS/Div
(PAL, NTSC)



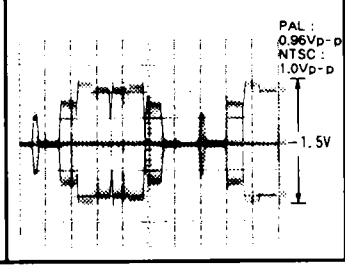
(16) -1/2
XD (at PAL)
V : 0.2V/Div H : 10 µS/Div
(PAL, NTSC)



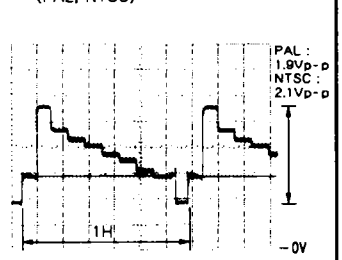
(16) -2/2
XD (at PAL)
V : 0.1V/Div H : 10nS/Div
(PAL, NTSC)



(26) COUT (at PAL)
V : 20mV/Div H : 10 µS/Div
(PAL, NTSC)

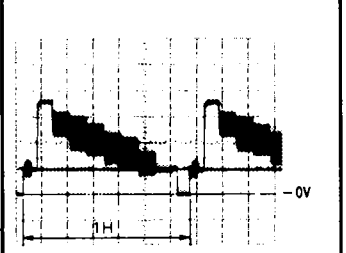


(27) YOUT (at PAL)
V : 50mV/Div H : 10 µS/Div
(PAL, NTSC)



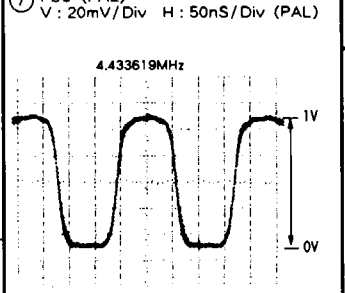
IC301 (CXD1171M)

(20) IO (PAL)
V : 50mV/Div H : 10 µS/Div (PAL)

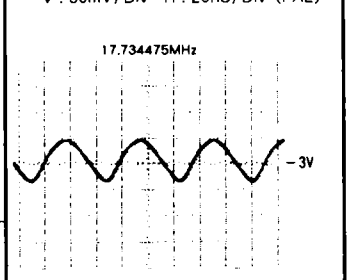


IC401 (MM1093PF)

(7) FSO (PAL)
V : 20mV/Div H : 50nS/Div (PAL)

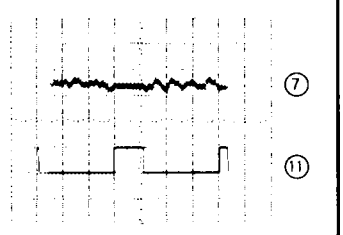


(14) 4FSC (PAL)
V : 50mV/Div H : 20nS/Div (PAL)



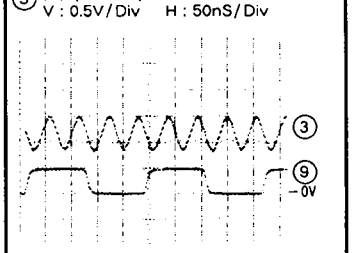
IC602 (TC74HC4053AF), IC603 (NJM082M)

(7) IC603 - pin 7 (PAL)
V : 10mV/Div H : 5mS/Div
(11) IC602 - pin 11 (PAL)
V : 0.5V/Div H : 5mS/Div



IC605 (TC74HC74AF)

(3) 1CLK (at PAL)
V : 0.1V/Div H : 50nS/Div
(9) 2Q (at PAL)
V : 0.5V/Div H : 50nS/Div



(3) PAL : 4.433619MHz
NTSC : 3.579545MHz

(9) PAL : 17.734475MHz
NTSC : 14.31818MHz

IC211 (MB90075PF-003)

Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	–	15	2
2	1.4	16	2.2
3	5	17	0
4	5	18	0
5	5	19	0
6	0	20	–
7	5	21	5
8	2.2	22	–
9	3	23	–
10	–	24	–
11	5	25	2.2
12	–	26	1.6
13	5	27	–
14	0	28	0

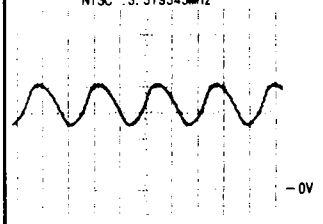
IC301 (CXD1171M)

Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	–	13	0
2	–	14	0
3	–	15	2.1
4	–	16	2.1
5	–	17	2.5
6	–	18	4
7	–	19	4
8	–	20	–
9	0	21	0
10	0	22	4
11	0.5	23	5
12	2.4	24	5

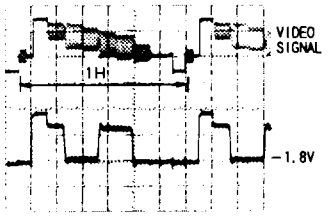
Note : (No.) in the table correspond to the pin number.
Values indicate the waveforms and voltages in the play mode.

IC701 (CXA1585Q)

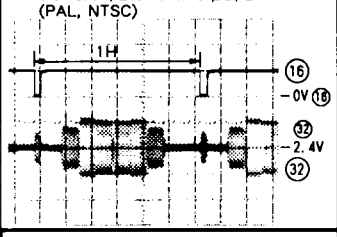
⑤ SC OUT (at PAL)
V : 50mV/Div H : 0.1 μS/Div
(PAL, NTSC)
PAL : 4.433619MHz
NTSC : 3.579545MHz



⑩ R OUT (at PAL)
V : 50mV/Div H : 10 μS/Div
(PAL, NTSC)

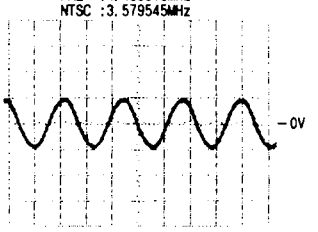


⑯ BF OUT (at PAL)
V : 0.5V/Div H : 10 μS/Div
(PAL, NTSC)
㉜ C IN (at PAL)
V : 10mV/Div H : 10 μS/Div
(PAL, NTSC)



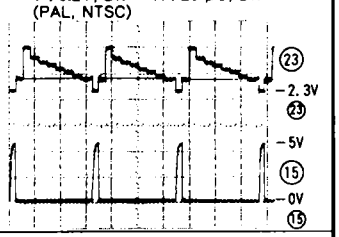
IC702 (CXA1645M)

⑥ SC IN
V : 20mV/Div H : 0.1 μS/Div
(PAL, NTSC)
PAL : 4.433619MHz
NTSC : 3.579545MHz



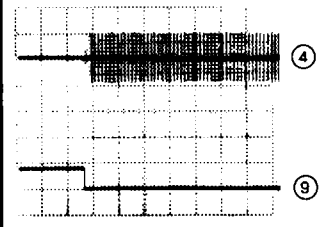
⑧ B OUT (at PAL)
V : 50mV/Div H : 10 μS/Div
(PAL, NTSC)

㉓ SYNC IN (at PAL)
V : 20mV/Div H : 20 μS/Div
(PAL, NTSC)
⑮ SYNC (at PAL)
V : 0.2V/Div H : 20 μS/Div
(PAL, NTSC)

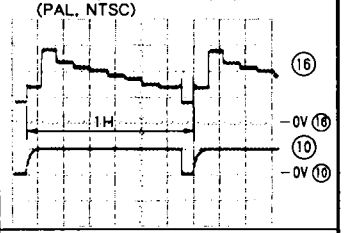


IC801 (BU4053BCF)

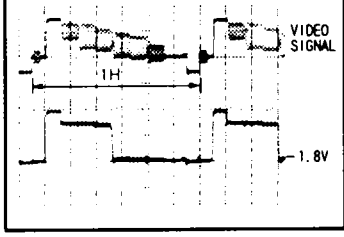
④ (PAL)
V : 50mV/Div H : 0.5mS/Div (PAL)
⑨ (PAL)
V : 0.5V/Div H : 0.5mS/Div (PAL)



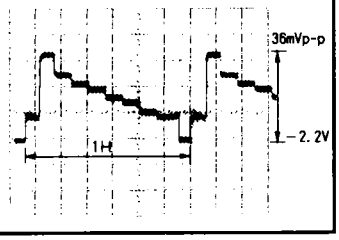
⑯ Y OUT
V : 0.1V/Div H : 10 μS/Div
(PAL, NTSC)
⑩ CSYNC
V : 0.5V/Div H : 10 μS/Div
(PAL, NTSC)



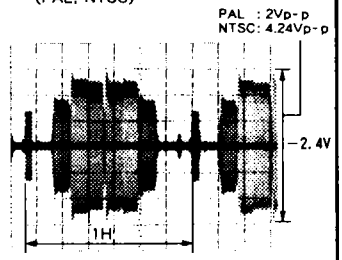
⑨ G OUT (at PAL)
V : 50mV/Div H : 10 μS/Div
(PAL, NTSC)



㉔ Y IN (at PAL)
V : 10mV/Div H : 10 μS/Div
(PAL, NTSC)



⑮ C OUT (at PAL)
V : 20mV/Div H : 10 μS/Div
(PAL, NTSC)



IC201 (CXD2024AQ)

Pin No.	Voltage (V)	Pin No.	Voltage (V)	Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	0	21	0	41	2.6	61	0
2	0	22	0.5	42	2.6	62	0
3	0	23	0	43	0	63	0
4	0	24	0	44	0	64	0
5	0	25	–	45	0	65	0
6	0	26	5	46	0	66	0
7	0	27	2.6	47	0	67	5
8	0	28	5	48	0	68	5
9	0	29	5	49	0	69	–
10	0	30	0	50	0	70	–
11	2.3	31	–	51	0	71	–
12	0	32	3.4	52	0	72	0
13	5	33	2.6	53	5	73	5
14	2.4	34	2.6	54	0	74	0
15	2.4	35	0	55	0	75	0
16	2.5	36	1.1	56	5	76	0
17	5	37	5	57	0	77	0
18	5	38	0	58	0	78	0
19	0	39	1.3	59	0	79	0
20	0	40	3.4	60	0	80	0

IC401 (MM1093PF)

Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	3.3	9	3.4
2	0.7	10	5
3	2.4	11	5
4	3.2	12	3.2
5	0	13	2
6	0	14	2.9
7	–	15	–
8	0	16	–

IC701 (CXA1585Q)

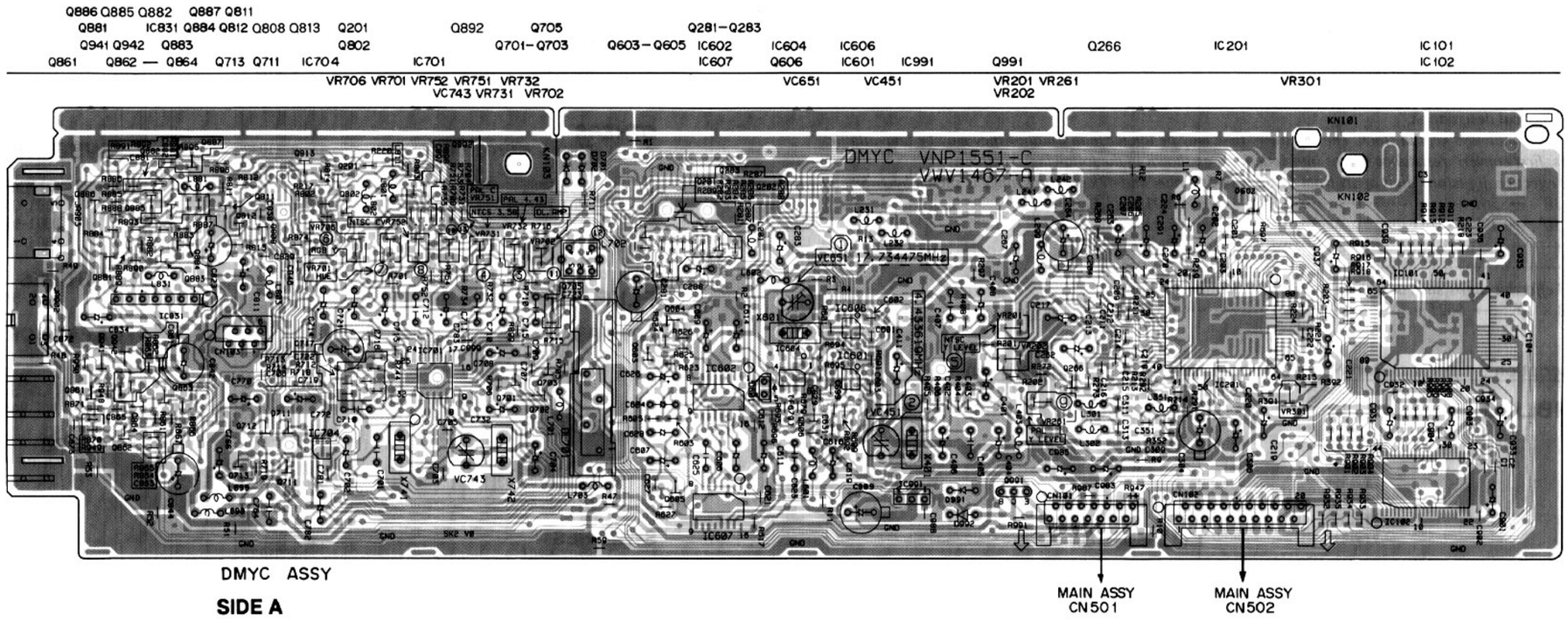
Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	2	17	3.1
2	3.4	18	3
3	3.1	19	2.5
4	3.2	20	3.1
5	1.6	21	3.1
6	0	22	4.2
7	5	23	2.5
8	2	24	2.5
9	2	25	5
10	2	26	0
11	0(NTSC) 2.3(PAL)	27	2.5
12	3.15	28	2.1
13	3.1	29	1.23
14	0(NTSC) 2.3(PAL)	30	2.5
15	H:4 over L:0.5 under	31	2.2
16	H:4 over L:0.5 under	32	2.3

IC702 (CXA1645M)

Pin No.	Voltage (V)	Pin No.	Voltage (V)
1	0 *	13	2
2	2(Black level at CLAMP)	14	4
3		15	2.2
4		16	1.3 (Black level)
5	–	17	1.6 (Black level)
6	–	18	2
7	1.7	19	5 *
8	H:3.6 L:3.2	20	1.2 (Black level)
9	2.5	21	1.7 (Black level)
10	2.2	22	
11	–	23	
12	5 *	24	0 *

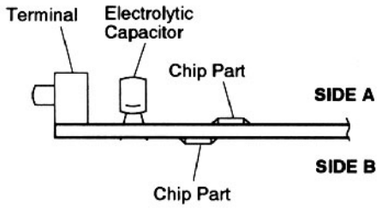
* : External apply voltage.

PCB – 3



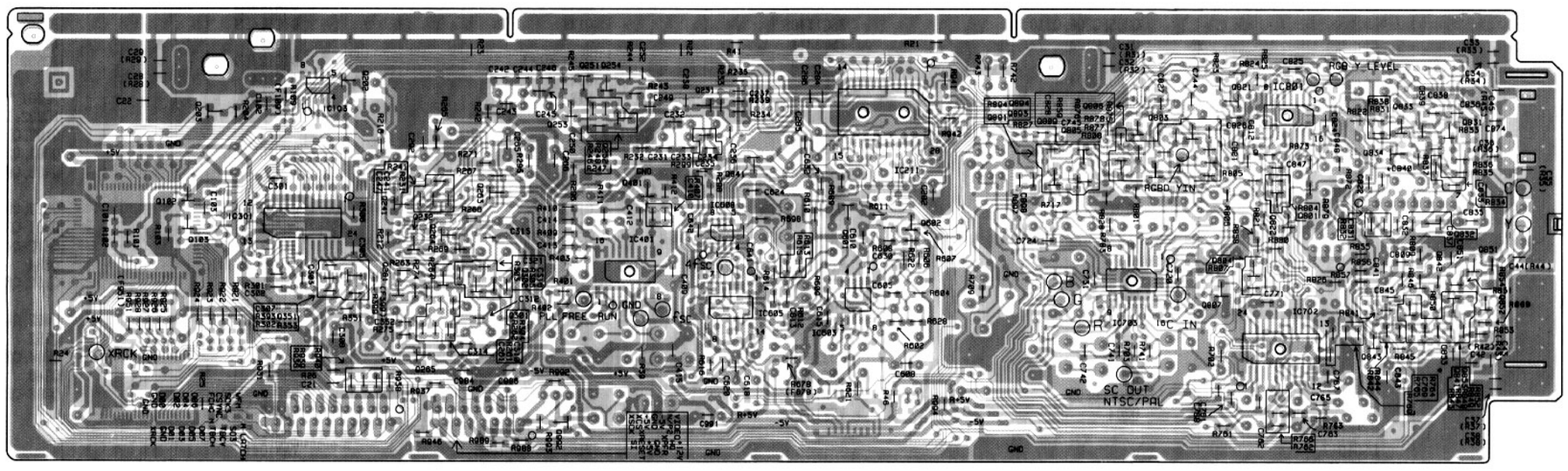
DMYC ASSY

SIDE A



- The pink colored is reverse side pattern.
- This PCB is double sided.

- The parts mounted on this PCB include all necessary parts for several destinations.
  For further information for respective destinations, be sure to check with the schematic diagram.
- Mounted position of the chip parts are showed as "—" or "⊤"



SIDE B

- The pink colored is reverse side pattern.
- This PCB is double sided.

4. PCB PARTS LIST

NOTES:

- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex.1 When there are 2 effective digits(any digit apart from 0), such as 560 ohm and 47k ohm(tolerance is shown by J=5%, and K=10%).

560Ω → 56 × 10¹ → 561 ····· RD1/4PU561J
47kΩ → 47 × 10¹ → 473 ····· RD1/4PU473J
0.5Ω → 0R5 ····· RN2H0R5K
1Ω → 1R0 ····· RS1P1R0K

Ex.2 When there are 3 effective digits(such as in high precision metal film resistors).

5 62kΩ → 562 × 10¹ → 5621 ····· RN1/4PC5621F

Mark	No.	Description	Part No.
LIST OF ASSEMBLIES			
NSP	MACB ASSY		VWM1535
NSP	├ PKSB ASSY		VWG1555
NSP	├ FG ASSY		VWG1556
NSP	├ TNSB ASSY		VWG1557
NSP	├ BISB ASSY		VWG1558
NSP	└ LMSB ASSY		VWG1612
⚠	SYPS ASSY		VWR1275
	FLKB ASSY		VWM1677
NSP	├ KEYB ASSY		VWG1728
	├ FLKY ASSY		VWG1743
	└ PWSB ASSY		VWG1744
NSP	MAIN ASSY		VWS1240
	DMYC ASSY		VWV1467
	SCRB ASSY		VWV1470
MACB ASSY			
OTHERS			
	PC Board MACB		VNP1479
PKSB ASSY			
SWITCHES			
	S104, S105		DSG1017
FG ASSY			
SEMICONDUCTOR			
	D101		GP1S24
TNSB ASSY			
SWITCH			
	S111		DSG1017
BISB ASSY			
SWITCH			
	S112		DSG1017
LMSB ASSY			
SWITCHES			
	S101-S103		DSG1017
OTHERS			
	CN101	12P FFC CONNECTOR	52044-1245
SYPS ASSY			
SEMICONDUCTORS			
⚠	IC201		HA17431P
⚠	IC210		ICP-N15
⚠	IC211		ICP-N20
	IC202		UPC358C
	Q207, Q208, Q214		2SA933S
	Q205, Q206, Q210		2SC1740S
⚠	Q102, Q103		2SC3377
⚠	Q213		2SD2395
	Q203, Q204		T7F4S
	Q201, Q202		T7F4T
⚠	Q209		VZF1040
⚠	Q101		VZF1041
⚠	D104		1SS270A
	D209-D212, D216		AG01Z-V0
⚠	D101		D2SB60F4004
⚠	D102		EG01C
⚠	D103		MTZJ2.7B
	D218		MTZJ8.2B
⚠	D200		PS2561L1-1VM
⚠	D106		RD18FB2
	D207		RD33FB2
⚠	D206		VZF1039
⚠	D202, D203		VZF1042
⚠	D204		VZF1043

Mark	No.	Description	Part No.
RESISTORS			
⚠	R257(68Ω, 1/4W)		VCN1048
⚠	R258(10Ω, 1/4W)		VCN1051
⚠	R256(0.22Ω, 1/2W))		VCN1055
OTHERS			
⚠	F101	FUSE(T1.6AH250V)	REK1033
⚠	F203	FUSE	VEK1033
⚠	F201, F202	FUSE	VEK1034
⚠	F204, F205	FUSE(1.0A/125V)	VEK1036
FLKB ASSY			
OTHERS			
	PC Board FLKB		VNP1557
KEYB ASSY			
SEMICONDUCTORS			
	D201, D202, D211, D212		SLR-342DUT31
	D221, D222		SLR-342DUT31
SWITCHES			
	S201-S204		ASG1034
RESISTORS			
	All Resistors		RD1/4PU□□□J
OTHERS			
	CN201	FJ CONNECTOR 6P	06R-FJ
FLKY ASSY			
SEMICONDUCTORS			
	IC102		AT93C46-10PC
	IC101		PD3337A
	IC141		S-806D
	Q142		DTA144ES
	Q141		DTC114ES
	Q181-Q184		DTC124ES
	D141		1SS254
	D181, D182		MPG3062X
SWITCHES			
	S101-S107		ASG1034
CAPACITORS			
	C142		CEAL100M16
	C101		CEAL470M6R3
	C111, C141		CKPUYF223Z25
	C143		CKPUYY103M16
RESISTORS			
	All Resistors		RD1/4PU□□□J
OTHERS			
	CN102	FJ CONNECTOR 6P	06P-FJ
	CN103	1.25FJ CONNECTOR 9P	09P-1.25FJ
	CN106	FFC BOTTOM CONNECTOR 16P	52492-1620
	X101	CERAMIC RESONATOR(8.0MHz)	EFOEC8004A4
	V101	FL TUBE	VAW1041

Mark	No.	Description	Part No.
		SPACER	VEC1599
		FL HOLDER	VNF1087
PWSB ASSY			
SEMICONDUCTORS			
	Q301, Q304, Q305		DTC124ES
	D301-D303		SLR-342MCT31
	D304		SLR-342VCT31
SWITCHES			
	S301-S303		ASG1034
CAPACITOR			
	C301		CEJA100M16
RESISTORS			
	All Resistors		RD1/4PU□□□J
OTHERS			
	CN301	1.25FJ CONNECTOR 9P	09R-1.25FJ
		REMOTE RECEIVER UNIT	GP1U28X
MAIN ASSY			
SEMICONDUCTORS			
	IC906		BA10393F
	IC803		LA6510
	IC400		LA7133
	IC901		LA9420M
	IC801		LA9425
	IC802		LC78681KE
⚠	IC203		NJM78L05A
⚠	IC206		NJM78M08FA
⚠	IC207		NJM79L08A
	IC351		PA0061AM
	IC101		PD0237A2
	IC500		PD6159A
	IC902		TA8410AK(V18)
	IC401, IC804		TC4W53F
	IC502		TC7SU04F
	IC201		TC9400F
	IC202, IC903, IC905		XRA4560F
	Q102, Q110, Q409, Q410, Q916		2PB709A
	Q201, Q202, Q321, Q322, Q324		2PD601A
	Q406, Q411, Q805, Q903, Q904		2PD601A
	Q907, Q908, Q915, Q917		2PD601A
	Q301-Q304, Q404, Q407, Q408		2SA1037K
	Q412-Q414, Q503		2SA1037K
	Q834		2SA854S
	Q162, Q213		2SA933S
	Q402, Q405, Q803		2SC2412K
	Q152		2SC3802K
	Q204, Q205		2SD2144S
	Q840		FMY1A
	Q208-Q212, Q323, Q403		UN2112

Mark	No.	Description	Part No.
	Q514, Q515, Q905, Q906, Q918		UN2112
	Q103, Q161, Q206, Q207, Q214		UN2212
	Q901, Q910		UN2212
	D202, D203		11EQS06
	D102, D162, D180, D205, D206		1SS254
	D301-D304, D401, D801		1SS254
	D901, D902, D905, D963		1SS254
	D171		1SS355
	D201		KV1851
	D161		MTZJ10B
	D110		MTZJ5.1B
	D802		UDZ2.0B

COILS AND FILTERS

	F503		DTF1069
	L510, L511		LAU101J
	L404, L405, L411		LAU120J
	L401		LAU121J
	L415		LAU180J
	L302, L802-L804		LAU181J
	L301, L408, L800, L801		LAU220J
	L403, L502		LAU270J
	L203		LAU2R2J
	L407		LAU330J
	L414		LAU390J
	L406, L501		LAU430J
	L402		LAU470J
	L410		LAU560J
	L412		LAU8R2J
	L409		LFA561J
	F301	684kHz B.P.FILTER	VTF1035
	F302	1066kHz B.P.FILTER	VTF1036
	F501	14.3MHz FILTER	VTF1055
	F502	15.0MHz FILTER	VTF1068

CAPACITORS

	C507, C524, C552	CCSQCH050C50
	C466, C474, C475, C809, C811	CCSQCH070D50
	C159, C411, C414, C418, C431	CCSQCH100D50
	C454, C510, C567	CCSQCH100D50
	C302, C412, C810, C846, C848	CCSQCH101J50
	C891, C944	CCSQCH101J50
	C472	CCSQCH120J50
	C413	CCSQCH121J50
	C517	CCSQCH150J50
	C161, C303, C446, C449, C812	CCSQCH151J50
	C248, C307, C429	CCSQCH180J50
	C203, C813, C950	CCSQCH220J50
	C162, C448, C584, C935	CCSQCH221J50
	C308, C415, C426, C428, C473	CCSQCH270J50
	C506, C931	CCSQCH270J50
	C280, C281	CCSQCH271J50
	C106, C107, C309, C427, C435	CCSQCH330J50
	C459, C511, C523, C551, C916	CCSQCH330J50
	C382	CCSQCH331J50
	C436	CCSQCH360J50
	C258-C263, C301, C402	CCSQCH390J50
	C232, C329, C441	CCSQCH470J50
	C383	CCSQCH471J50
	C439	CCSQCH560J50
	C310, C403, C522, C806	CCSQCH680J50

Mark	No.	Description	Part No.
	C304, C814		CCSQCH820J50
	C440		CCSQCH910J50
	C450, C833, C836, C844		CEAL470M6R3
	C850		CEAL4R7M50
	C434, C838		CEALNP470M6R3
	C972		CEANP220M16
	C227, C286, C904		CEAS010M50
	C228, C367, C444, C917		CEAS100M50
	C364, C424, C565		CEAS101M10
	C171, C274, C275, C465, C922		CEAS220M25
	C967		CEAS220M25
	C519, C532, C576, C974, C975		CEAS221M10
	C845, C870, C902, C926		CEAS2R2M50
	C101, C207, C225, C226		CEAS470M10
	C270, C271, C363, C369, C370		CEAS470M10
	C422, C458, C508, C516, C527		CEAS470M10
	C530, C553, C555, C562, C564		CEAS470M10
	C569, C801, C803, C842, C893		CEAS470M10
	C927, C933		CEAS470M10
	C210, C216		CEAS471M10
	C368, C913, C943		CEASR47M50
	C968, C987		CEHAQ220M50
	C895		CEJA101M6R3
	C149, C150, C220-C224, C233		CKSQYB102K50
	C377, C421, C525, C907, C914		CKSQYB102K50
	C936		CKSQYB102K50
	C981		CKSQYB104K25
	C919		CKSQYB332K50
	C361, C362		CKSQYB392K50
	C355-C358, C909		CKSQYB472K50
	C110, C122, C160, C196-C198		CKSQYF103Z50
	C201, C202, C205, C208, C211		CKSQYF103Z50
	C213, C305, C306, C311, C312		CKSQYF103Z50
	C371-C373, C376, C407, C410		CKSQYF103Z50
	C419, C420, C432, C433		CKSQYF103Z50
	C437, C438, C445, C447, C457		CKSQYF103Z50
	C460, C463, C464, C478, C479		CKSQYF103Z50
	C509, C512-C514, C518		CKSQYF103Z50
	C520, C521, C526, C528, C529		CKSQYF103Z50
	C566, C579-C583, C585, C586		CKSQYF103Z50
	C802, C804, C807, C827, C828		CKSQYF103Z50
	C834, C835, C843, C876, C888		CKSQYF103Z50
	C892, C894, C896, C918		CKSQYF103Z50
	C928, C929, C932, C937-C939		CKSQYF103Z50
	C941, C961, C962, C964, C971		CKSQYF103Z50
	C982		CKSQYF103Z50
	C102, C103, C151, C209, C215		CKSQYF104Z25
	C284, C285, C321, C365, C366		CKSQYF104Z25
	C423, C425, C443, C451		CKSQYF104Z25
	C461, C462, C468, C471, C505		CKSQYF104Z25
	C515, C533, C554, C561, C563		CKSQYF104Z25
	C568, C570, C571, C831, C832		CKSQYF104Z25
	C840, C841, C847, C872-C874		CKSQYF104Z25
	C910-C912, C940, C983		CKSQYF104Z25
	C837, C921, C930		CKSQYF223Z50

Mark	No.	Description	Part No.
	C359, C360, C905, C951		CKSQYF224Z25
	C442, C590, C591, C808, C815		CKSQYF473Z25
	C875, C877, C924, C925		CKSQYF473Z25
	C942		CQMA103J50
	C920		CQMA104J50
	C455, C908, C960		CQMA154J50
	C278, C282		CQMA182J50
	C903		CQMA222J50
	C923		CQMA473J50
	C934		CQMA681J50
	C456		CQMA683J50
	C871	(10μF/10V)	VCH1152
	VC501, VC503	(20pF)	VCM-008

RESISTORS

	R414		RD1/4PU470J
	R162		RD1/4PU471J
⚠	R220, R222		RFA1/6PU4R7J
	R987, R989		RN1/10SE103D
	R986, R990		RN1/10SE333D
	R554		RN1/10SE391D
	R259-R262		RN1/10SE473D
	VR450	(2.2kΩ)	RCP1019
	VR603	(4.7kΩ)	RCP1020
	VR604, VR607, VR608, VR612	(47kΩ)	RCP1047
	Other Resistors		RS1/10S□□□J

OTHERS

	CN108	12P FFC CONNECTOR	52045-1245
	CN121	16P FFC CONNECTOR	52045-1645
	CN102	21P FFC CONNECTOR	52045-2145
	CN103	23P FFC CONNECTOR	52233-2310
	CN106	11P TOP POST	B11P-SHF-1AA
	CN501	B TO B CONNECTOR 14P	BTFN14S-3SB7
	CN502	B TO B CONNECTOR 20P	BTFN20S-3SB7
	JA8	OPTICAL OUTPUT MODULE	GP1F32T
	JA3, JA4	REMOTE CONTROL JACK	RKN1004
		PCB BINDER	VEF1040
	JA6	2P PIN JACK	VKB1031
	JA1	1P PIN JACK	VKB1077
		SCREW TERMINAL	VNE1948
		EARTH METAL	VNF1084
	X101	CERAMIC RESONATOR(9.00MHz)	VSS1040
	X501	CRYSTAL RESONATOR (14.31818MHz)	VSS1073
	X503	CRYSTAL RESONATOR(15.0MHz)	VSS1079
	X201	CRYSTAL RESONATOR (16.9344MHz)	VSS1081

DMYC ASSY

SEMICONDUCTORS

	IC801	BU4053BCF
	IC701	CXA1585Q
	IC702	CXA1645M
	IC301	CXD1171M
	IC201	CXD2024AQ
	IC703	HD74HC4053FP
	IC102	HM530281RTT-25
	IC211	MB90075PF-003
	IC401	MM1093PF
	IC603	NJM082M

Mark	No.	Description	Part No.
	IC991		NJM78M05FA
	IC101		PD4596A
	IC831		TA7302P
	IC103, IC608		TC4W53F
	IC607		TC74HC221AF
	IC602		TC74HC4053AF
	IC605		TC74HC74AF
	IC601		TC7S86F
	IC606		TC7SU04F
	IC604		TC7WU04F
	Q201, Q251, Q253, Q254, Q264		2PB709A
	Q351, Q603-Q606, Q805, Q831		2PB709A
	Q834, Q843, Q853, Q864, Q881		2PB709A
	Q883-Q887, Q891		2PB709A
	Q231, Q232, Q241, Q252, Q261		2PD601A
	Q263, Q265, Q266, Q281-Q283		2PD601A
	Q301, Q302, Q401, Q601, Q705		2PD601A
	Q801-Q803, Q806, Q808		2PD601A
	Q811, Q812, Q821, Q822, Q833		2PD601A
	Q841, Q842, Q851, Q852		2PD601A
	Q861-Q863, Q882, Q892		2PD601A
	Q991		2SB1237X
	Q103, Q602, Q701, Q711, Q804		DTA124EK
	Q809, Q832, Q893		DTA124EK
	Q102, Q202, Q702, Q703		DTC124EK
	Q712, Q713, Q807, Q813, Q894		DTC124EK
	Q992		DTC124EK
	D991		11EQS06
	D992		1SR35-100AVL
	D701, D702		1SS254
	D602, D711		DAP202K
	D601		SVC201SPA

COILS

	L702	DTL1001
	L898	LAU100J
	L299, L899	LAU101J
	L231, L232, L241, L242	LAU150J
	L301, L302	LAU150J
	L602	LAU1R0J
	L351, L601, L802	LAU220J
	L403	LAU270J
	L281	LAU330J
	L831, L881	LAU470J
	L803	LAU820J
	L701	LAU8R2J
	L811	LFA220J

CAPACITORS

	C624	CCSQCH040C50
	C763	CCSQCH050C50
	C232, C243, C311, C412	CCSQCH060D50
	C845	CCSQCH100D50
	C745, C881	CCSQCH101J50
	C829	CCSQCH120J50
	C287, C840	CCSQCH150J50
	C285, C286	CCSQCH180J50
	C352	CCSQCH181J50
	C351	CCSQCH200J50

Mark	No.	Description	Part No.
	C224, C231, C234, C242, C245		CCSQCH220J50
	C310, C313		CCSQCH220J50
	C627, C723, C872-C874, C899		CCSQCH221J50
	C744		CCSQCH240J50
	C882		CCSQCH270J50
	C261, C415		CCSQCH330J50
	C235, C246, C314, C765		CCSQCH390J50
	C414		CCSQCH391J50
	C402, C631, C632, C641, C827		CCSQCH470J50
	C724		CCSQCH471J50
	C233, C244, C312, C620, C897		CCSQCH560J50
	C413		CCSQCH561J50
	C606		CEANP010M50
	C628, C702		CEANP100M25
	C604		CEANP2R2M50
	C713		CEAS010M50
	C770		CEAS100M50
	C288, C983, C985		CEAS101M10
	C626, C714, C721		CEAS220M25
	C262, C406, C811		CEAS2R2M50
	C834		CEAS330M16
	C202, C217, C219, C221, C263		CEAS470M10
	C267, C270, C283, C291, C306		CEAS470M10
	C401, C411, C607, C609, C611		CEAS470M10
	C614, C619, C704, C732		CEAS470M10
	C766, C772, C783		CEAS470M10
	C901, C931, C935		CEAS470M10
	C717, C823, C842, C844, C989		CEAS471M6R3
	C404, C408, C708, C710		CEAS4R7M50
	C264, C281, C304		CEHAQ471M10
	C623		CFTXA334J50
	C625, C718		CFTXA474J50
	C201, C223		CKSQYB102K50
	C605		CKSQYB222K50
	C204, C207, C403, C409, C410		CKSQYF103Z50
	C602, C613, C615, C630		CKSQYF103Z50
	C705-C707, C716, C719, C720		CKSQYF103Z50
	C722, C767, C771, C828		CKSQYF103Z50
	C830-C833, C988, C991		CKSQYF103Z50
	C102, C103, C203, C206, C209		CKSQYF104Z25
	C211-C216, C218, C220, C222		CKSQYF104Z25
	C236-C238, C241, C247		CKSQYF104Z25
	C249, C250, C252, C265, C266		CKSQYF104Z25
	C282, C284, C292, C301-C303		CKSQYF104Z25
	C305, C307-C309, C315, C316		CKSQYF104Z25
	C321, C601, C603, C608, C610		CKSQYF104Z25
	C612, C616, C618, C621, C629		CKSQYF104Z25
	C642, C709, C731, C761, C762		CKSQYF104Z25
	C768, C769, C812, C821, C822		CKSQYF104Z25
	C824-C826, C835-C839, C841		CKSQYF104Z25
	C843, C846-C848, C851, C853		CKSQYF104Z25
	C861, C863, C865, C902, C904		CKSQYF104Z25
	C932, C934, C936, C938, C984		CKSQYF104Z25
	C986		CKSQYF104Z25
	C22, C28, C3, C37		CKSQYF473Z25

Mark	No.	Description	Part No.
	C407		CQMA102J50
	C405, C701		CQMA103J50
	C764		CQMA104J50
	C711, C712, C715		CQMA473J50
	C903 (47μF)		RCH1139
	VC651 (20pF)		VCM-008
	VC451 (45pF/10V)		VCM1002

RESISTORS

	R287		RN1/10SE102D
	R731, R733		RN1/10SE133D
R765	RN1/10SE163D		
	R713, R732, R734		RN1/10SE273D
	R769		RN1/10SE392D
	R284		RN1/10SE562D
	R282, R285		RN1/10SE911D
	VR261	(1kΩ)	VCP1105
	VR731, VR732	(2.2kΩ)	VCP1107
	VR201, VR702, VR706	(4.7kΩ)	VCP1109
	VR701	(10kΩ)	VCP1111
	VR751, VR752	(22kΩ)	VCP1113
	Other Resistors		RS1/10S□□□J

OTHERS

	CN101	B TO B CONNECTOR 14P	BTFN14P-3RD7
	CN102	B TO B CONNECTOR 20P	BTFN20P-3RD7
	DL701	64μsec DELAY LINE	DTF1033
	JA903	1P PIN JACK	VKB1090
	JA902	4P MINI DIN SOCKET	VKN1072
		SCREW TERMINAL	VNE1948
	X601	CRYSTAL RESONATOR(17.734MHz)	VSS1059
	X401	CRYSTAL RESONATOR (4.433619MHz)	VSS1090
	X742	CRYSTAL RESONATOR (4.433619MHz)	VSS1091
	X741	CRYSTAL RESONATOR (3.579545MHz)	VSS1092

SCRB ASSY

SEMICONDUCTORS

D101		1SS353
D102, D103		UDZ5.6B

RELAYS

RY101-RY103	VSR-005

CAPACITORS

C101-C104	CCSQCH391J50
C106, C108, C110, C112, C114	CKSQYB102K50
C105, C107, C109, C111, C113	CKSQYF104Z25

RESISTORS

All Resistors	RS1/10S□□□J

OTHERS

	PCB BINDER	VEF1040
JA101	RGB CONNECTOR	VKB1056
	EARTH PLATE	VNF1097

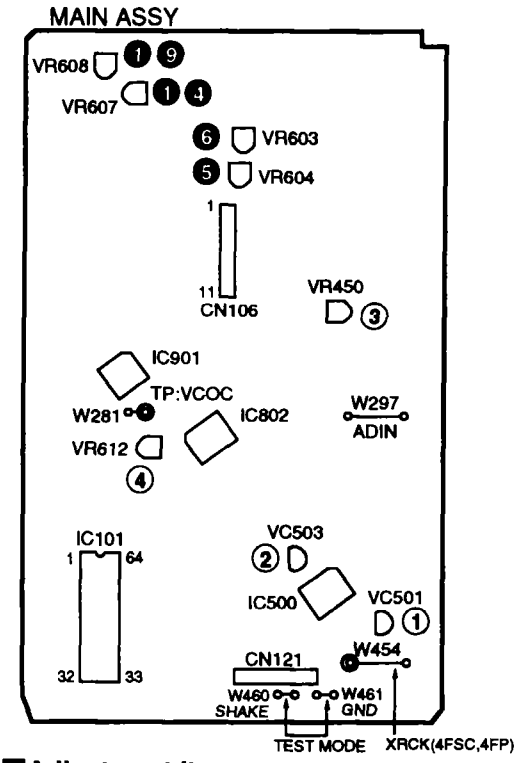
5. ADJUSTMENTS (調整方法)

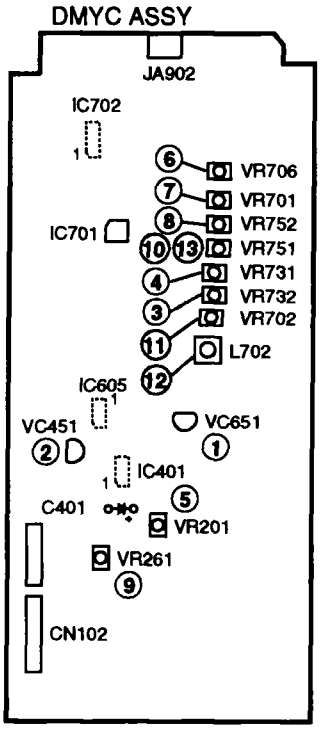
CAUTION

This player has the switching regulator system of the primary side.
If the power switch is turned to OFF, remove the disc, then the power switch is sure to turn to OFF after the blink of "LD" and "CD" indicators are finished.

5.1 ADJUSTMENT ITEMS AND LOCATION (調整項目と調整位置)

■Adjustment Points (PCB Part)





■Adjustment Items

[Mechanical Part]

❶ Tilt Offset Adjustment
(チルトオフセット調整)
❷ Tangential Direction Angle Adjustment for Side A
(A面タンジェンシャル傾き調整)
❸ Spindle Motor Centering Adjustment for Side A
(A面スピンドル芯出し調整)
❹ Crosstalk Check and Fine Tilt Offset Adjustment for Side A
(A面クロストーク確認及び、チルトオフセット微調)
❺ Focus Servo Loop Gain Adjustment
(フォーカスサーボループゲイン調整)
❻ Tracking Servo Loop Gain Adjustment
(トラッキングサーボループゲイン調整)
❼ Tangential Direction Angle Adjustment for Side B
(B面タンジェンシャル傾き調整)
❽ Spindle Motor Centering Adjustment for Side B
(B面スピンドル芯出し調整)
❾ Crosstalk Check and Fine Tilt Offset Adjustment for Side B
(B面クロストーク確認及び、チルトオフセット微調)

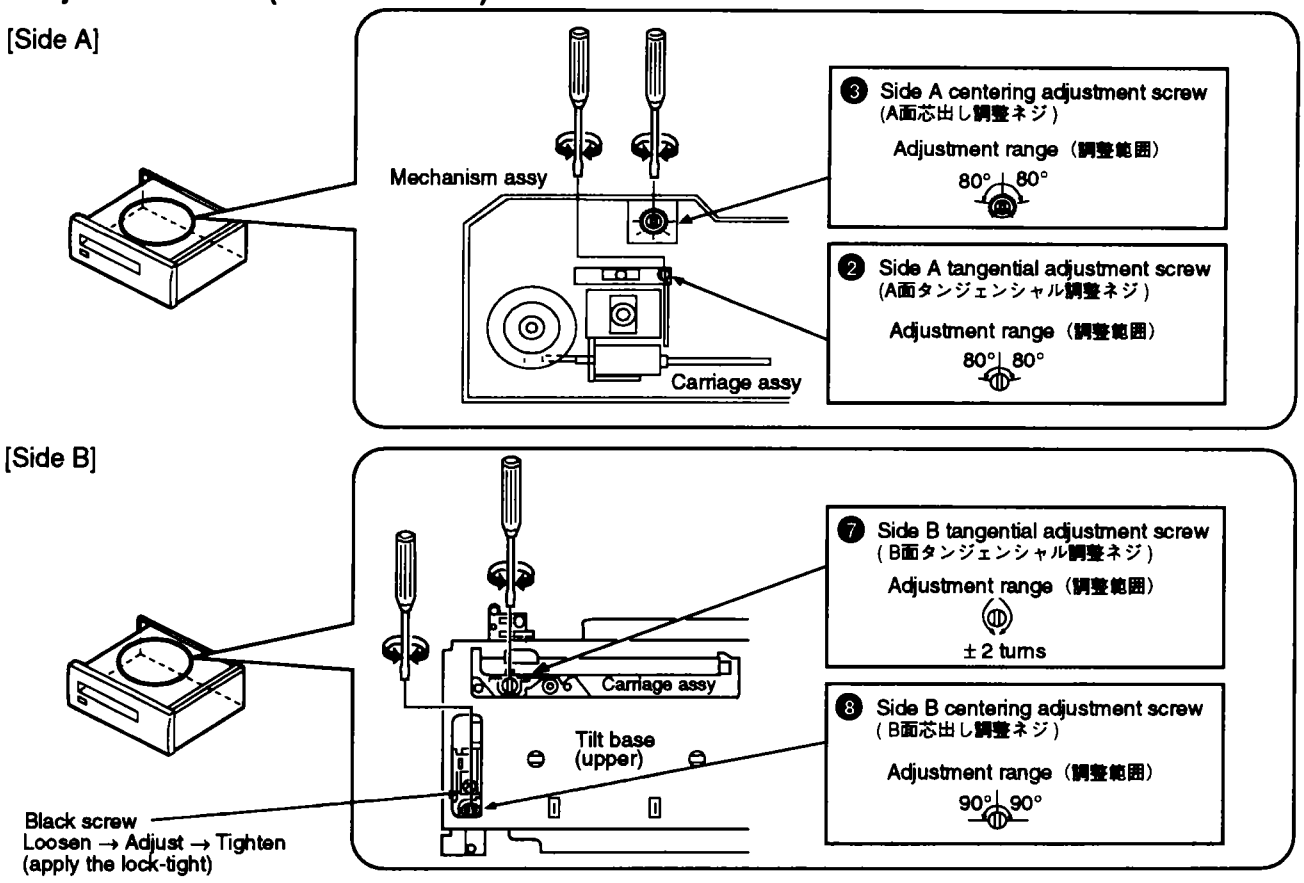
[Electrical Part of MAIN Assy]

① NTSC Master Clock Adjustment
(NTSCマスタークロック調整)
② PAL Master Clock Adjustment
(PALマスタークロック調整)
③ Output Video Level Adjustment
(出力ビデオレベル調整)
④ PLL Offset Adjustment
(PLLオフセット調整)

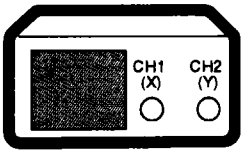
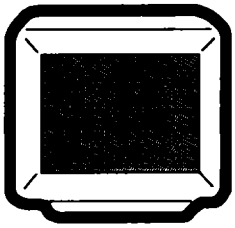
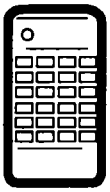
[Electrical Part of DMYC Assy]

① 17MHz Free-run Frequency Adjustment
(17MHzフリーラン周波数調整)
② 4.43MHz Free-run Frequency Adjustment for Y/C Separation
(Y/C分離用4.43MHzフリーラン周波数調整)
③ PAL 4.43MHz Free-run Frequency Adjustment for RGB Decoder
(RGBデコーダ用 PAL 4.43MHzフリーラン周波数調整)
④ NTSC 3.58MHz Free-run Frequency Adjustment for RGB Decoder
(RGBデコーダ用 NTSC 3.58MHzフリーラン周波数調整)
⑤ NTSC Y Level Adjustment
(NTSC Yレベル調整)
⑥ RGB Decoder Y Level Adjustment
(RGBデコーダYレベル調整)
⑦ RGB Decoder HUE Adjustment
(RGBデコーダHUE調整)
⑧ RGB Decoder NTSC Chroma Level Adjustment
(RGBデコーダNTSCクロマレベル調整)
⑨ PAL Y Level Adjustment
(PAL Yレベル調整)
⑩ Coarse RGB Decoder PAL Chroma Level Adjustment
(RGBデコーダPALクロマレベル粗調整)
⑪ RGB Decoder PAL Delay Line Amp Gain Adjustment
(RGBデコーダPALディレーラインアンプゲイン調整)
⑫ RGB Decoder PAL DAT Adjustment
(RGBデコーダPAL DAT調整)
⑬ Fine RGB Decoder PAL Chroma Level Adjustment
(RGBデコーダPALクロマレベル微調整)

■Adjustment Points (Mechanism Part)

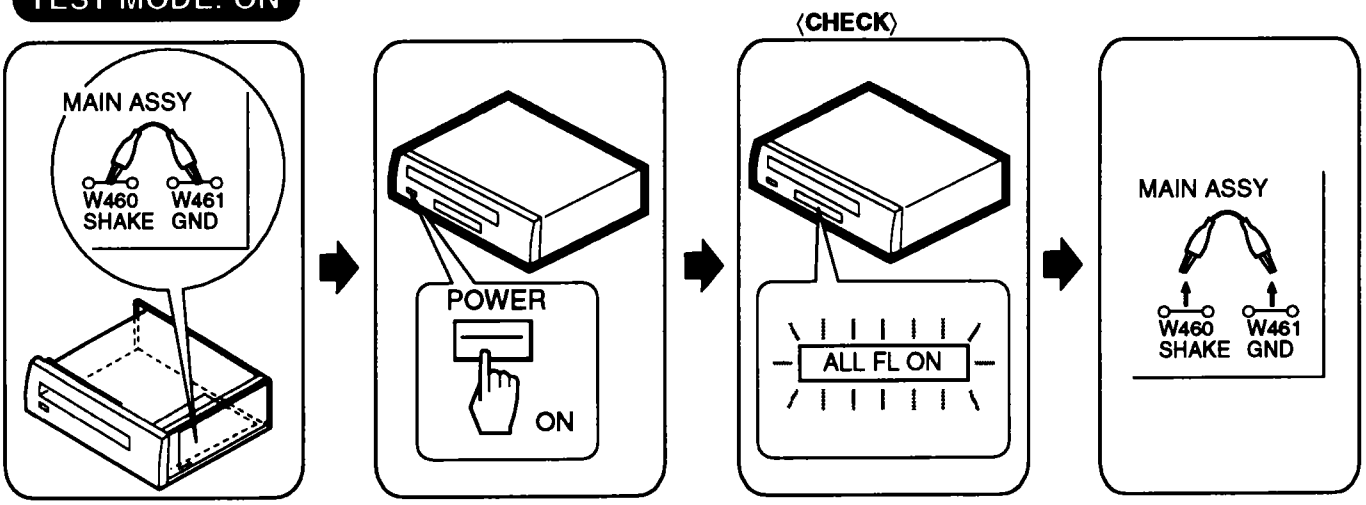


5.2 JIGS AND MEASURING INSTRUMENTS (調整に必要な治工具類)

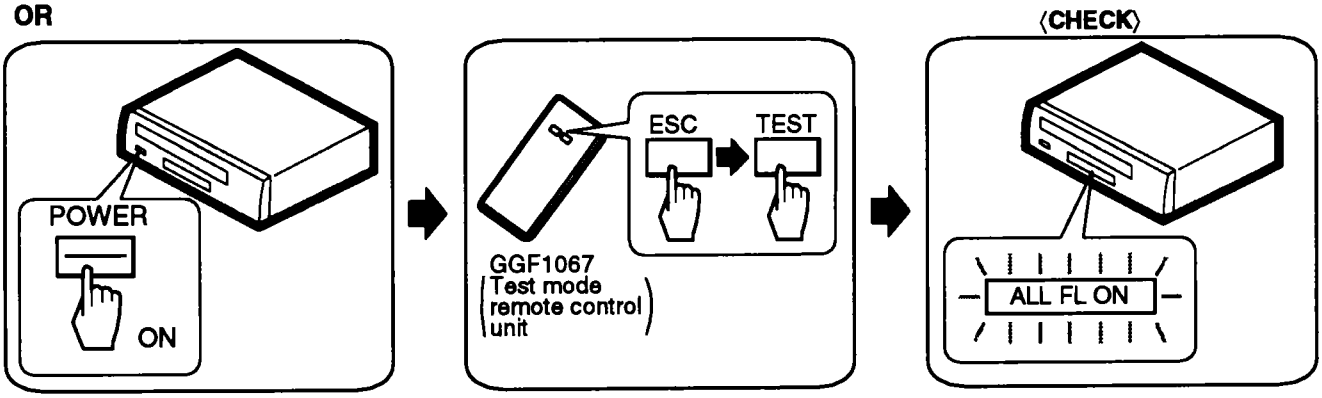
CD test disc (YEDS-7)	LD test disc NTSC disc (GGV1012) PAL disc (GGV1007)	⊖ Screwdriver (medium)	⊖ Screwdriver (small)
⊖ Precise screwdriver	⊕ Screwdriver (large)	⊕ Screwdriver (medium)	 Dual-trace oscilloscope (with delay) Frequency band ≧ 40MHz
Frequency counter Display digit ≧ 8-digit	 TV monitor	 Test mode remote control unit (GGF1067)	⊖ Plastic (or Celamic) screwdriver

5.3 TEST MODE (テストモード)

TEST MODE: ON

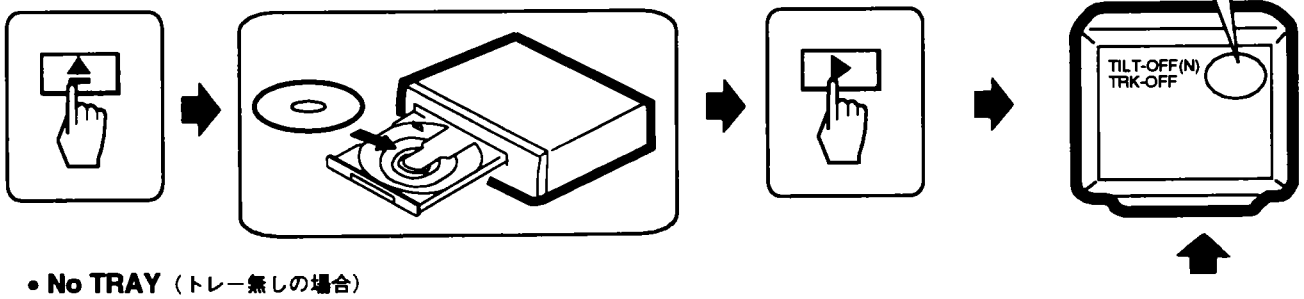


OR

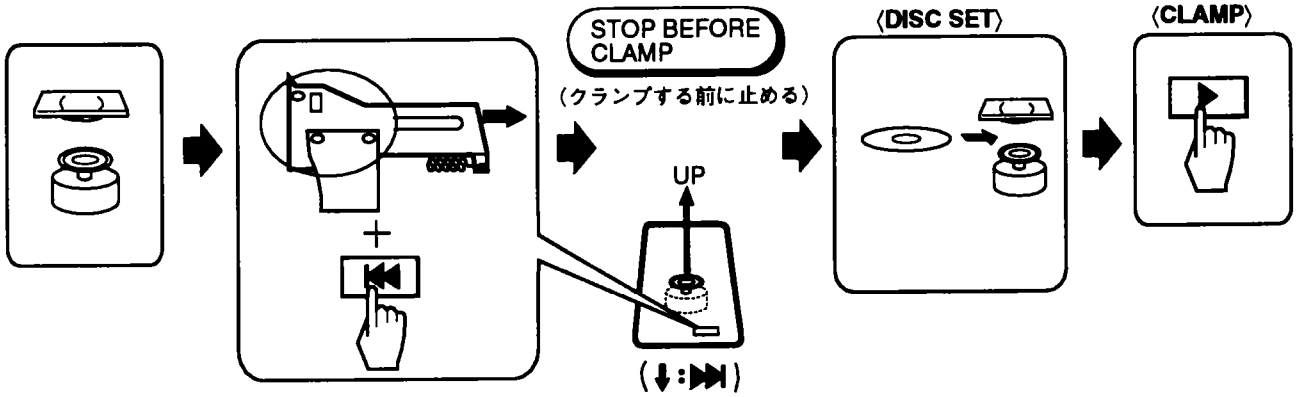


TEST MODE: DISC SET

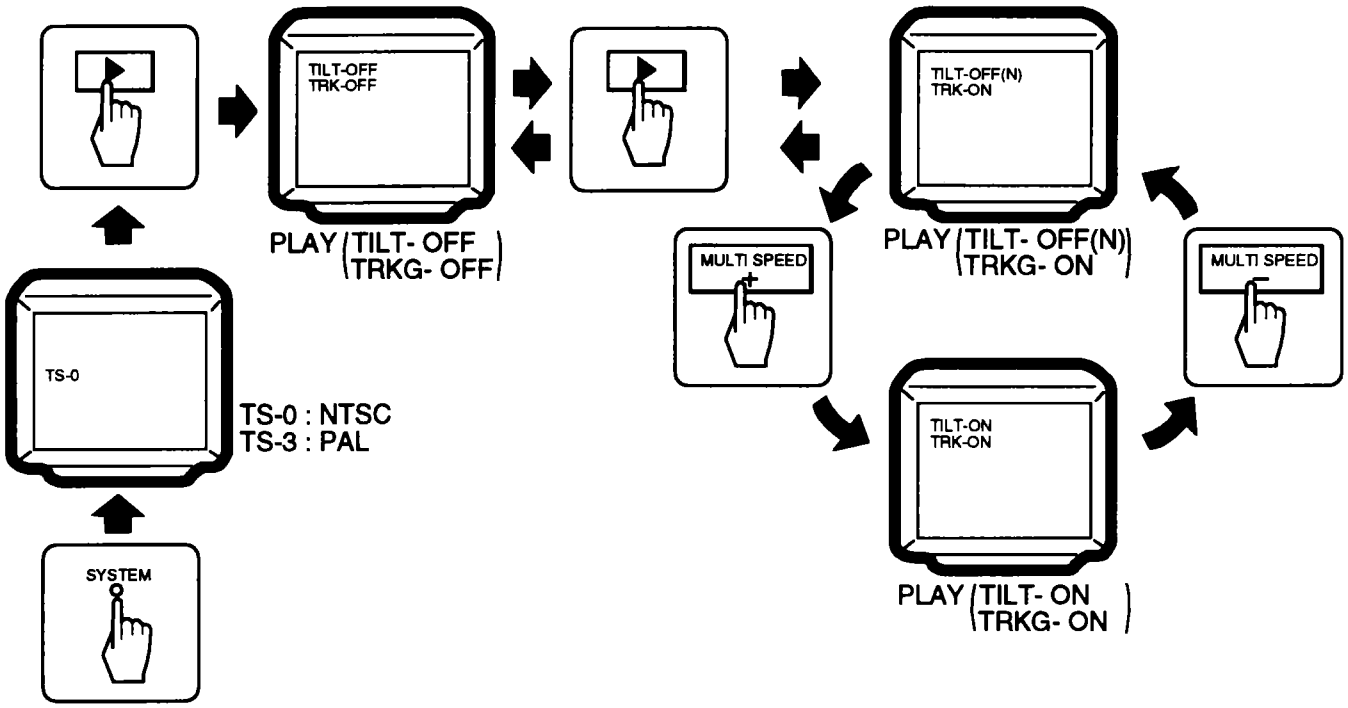
• **With TRAY** (トレー有りの場合)



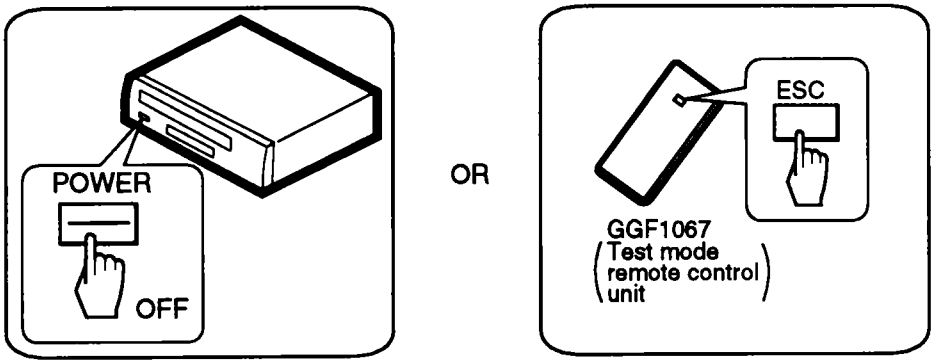
• **No TRAY** (トレー無しの場合)



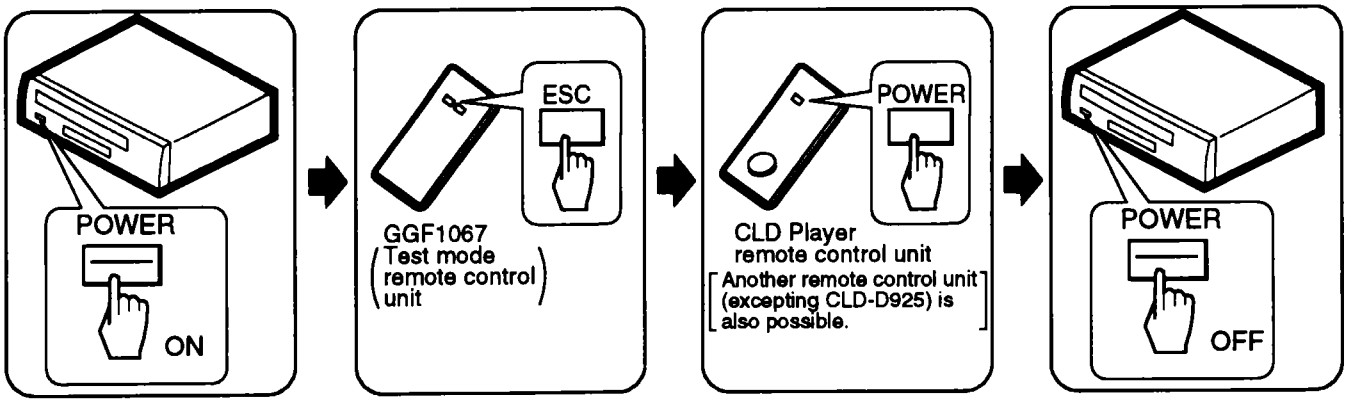
TEST MODE: PLAY



TEST MODE: OFF



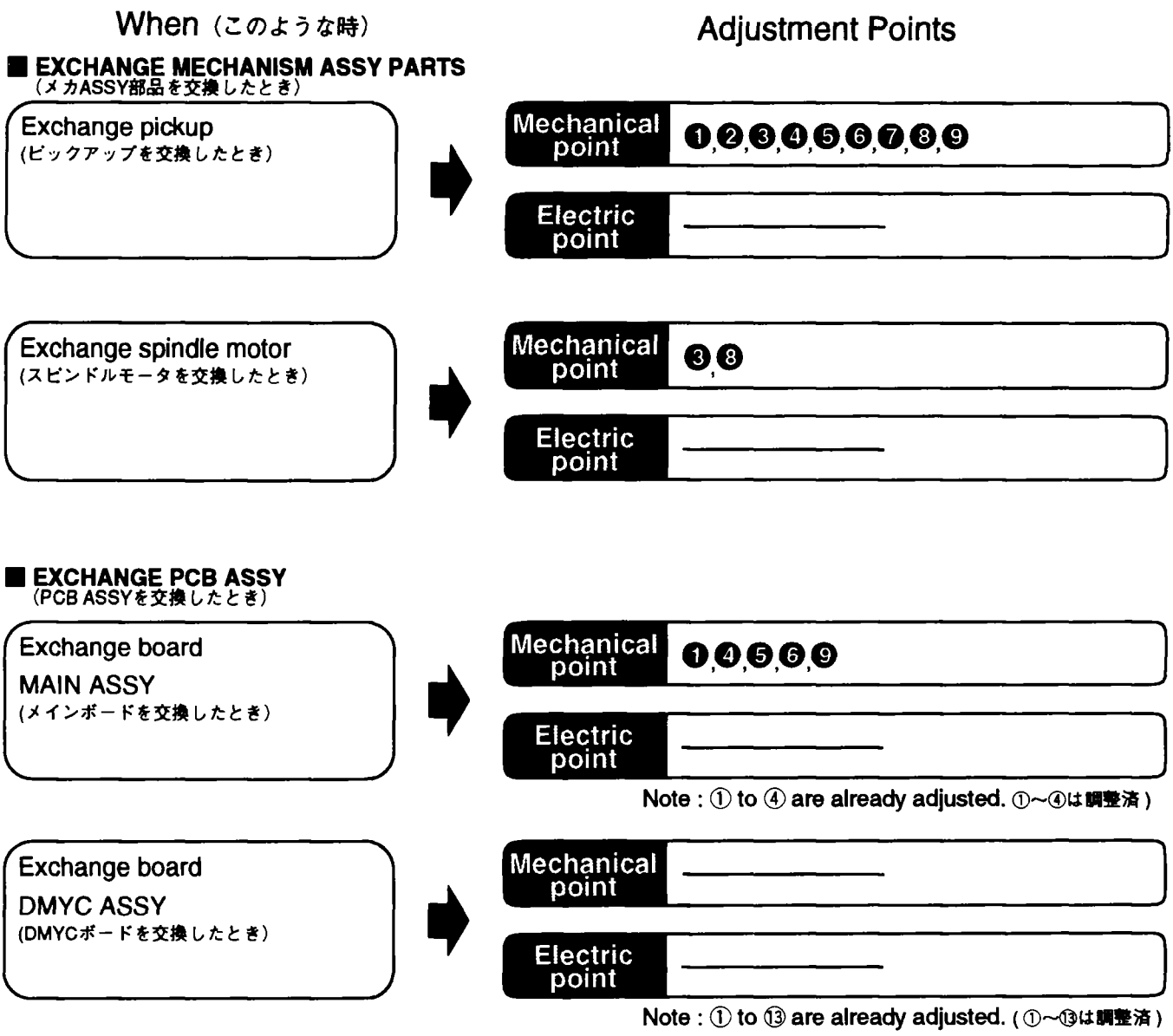
5.4 INITIALIZE METHOD OF EEPROM (EEPROMの初期化)



Storage functions and initial states in the EEPROM are as follows.

QUICK TURN : ON	SYSTEM : PAL (BLUE BACK)
DISPLAY OFF : OFF	LANGUAGE : ENGLISH
HQ CIRCUIT : ON	ERROR CODE : Refer to pages 62, 63 and 64

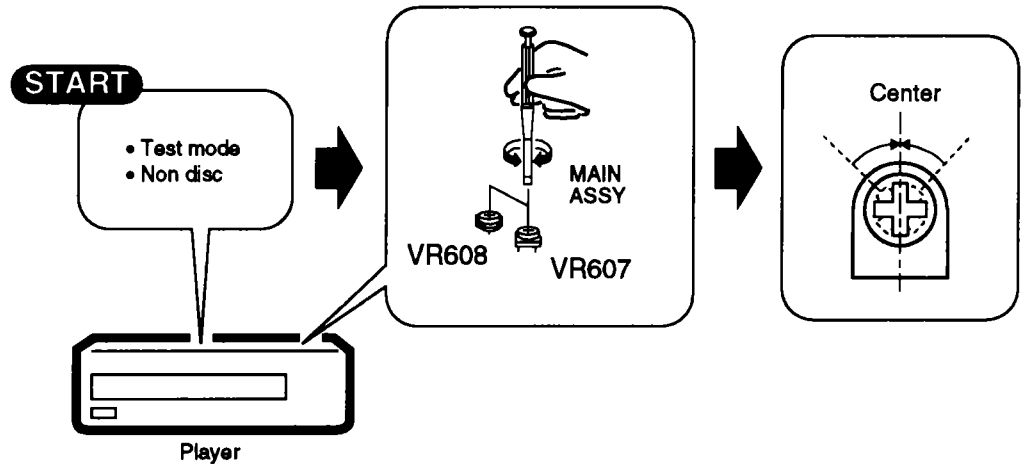
5.5 NECESSARY ADJUSTMENT POINTS (必要な調整項目)



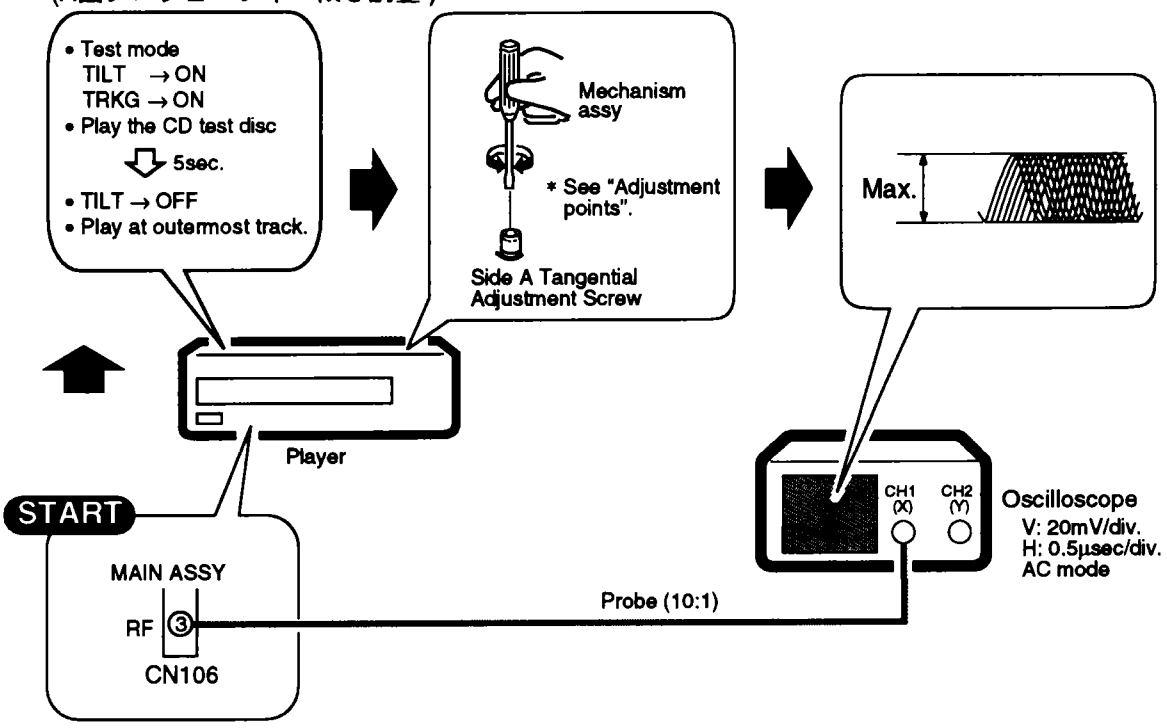
5.6 MECHANICAL ADJUSTMENT (機構系の調整)

(Be sure to use a NTSC test disc)

1 Tilt Offset Adjustment
(チルトオフセット調整)

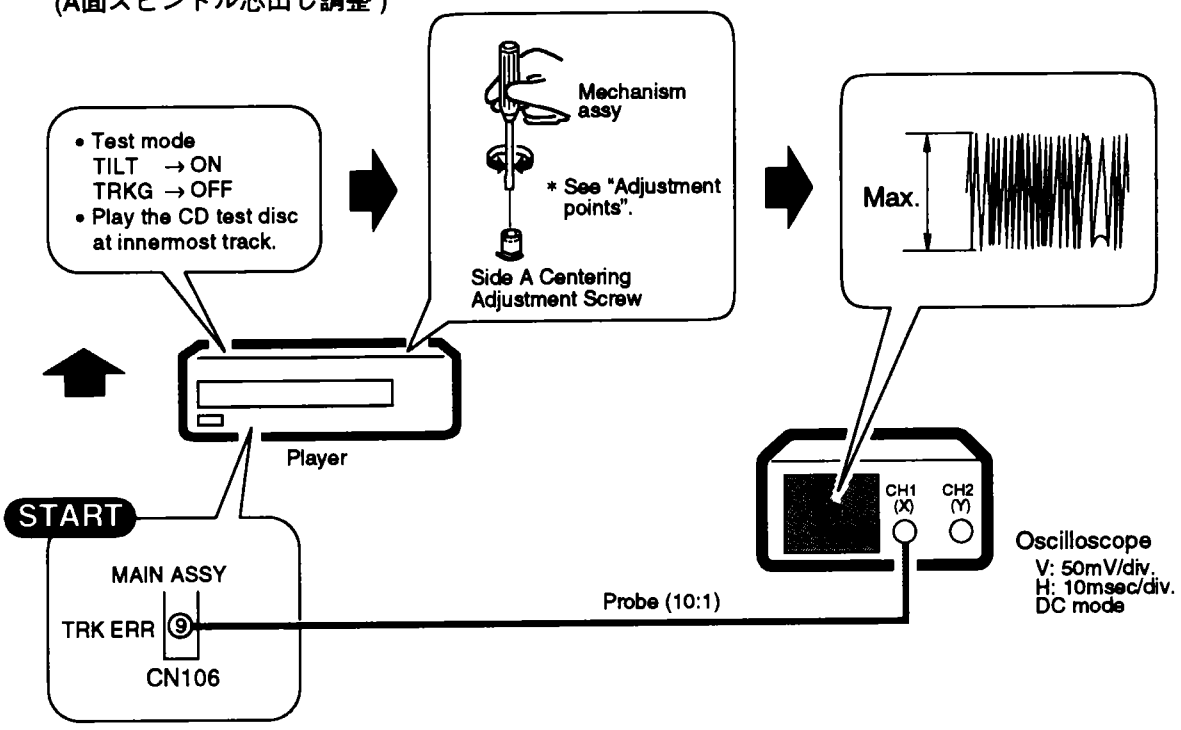


2 Tangential Direction Angle Adjustment for Side A
(A面タンジェンシャル傾き調整)



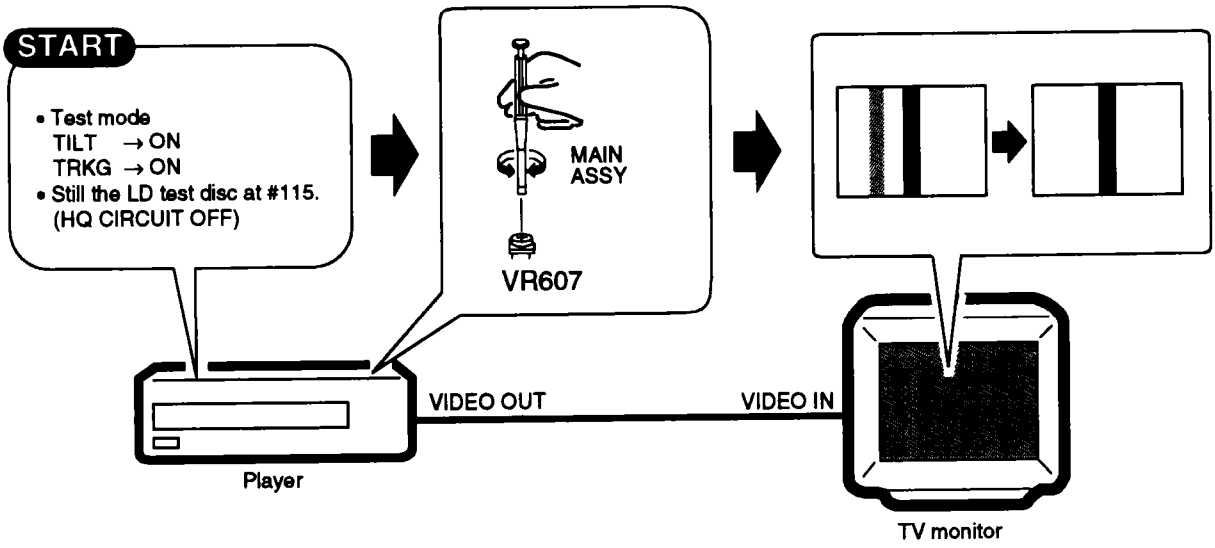
outermost : 最外周

❸ Spindle Motor Centering Adjustment for Side A
(A面スピンドル芯出し調整)

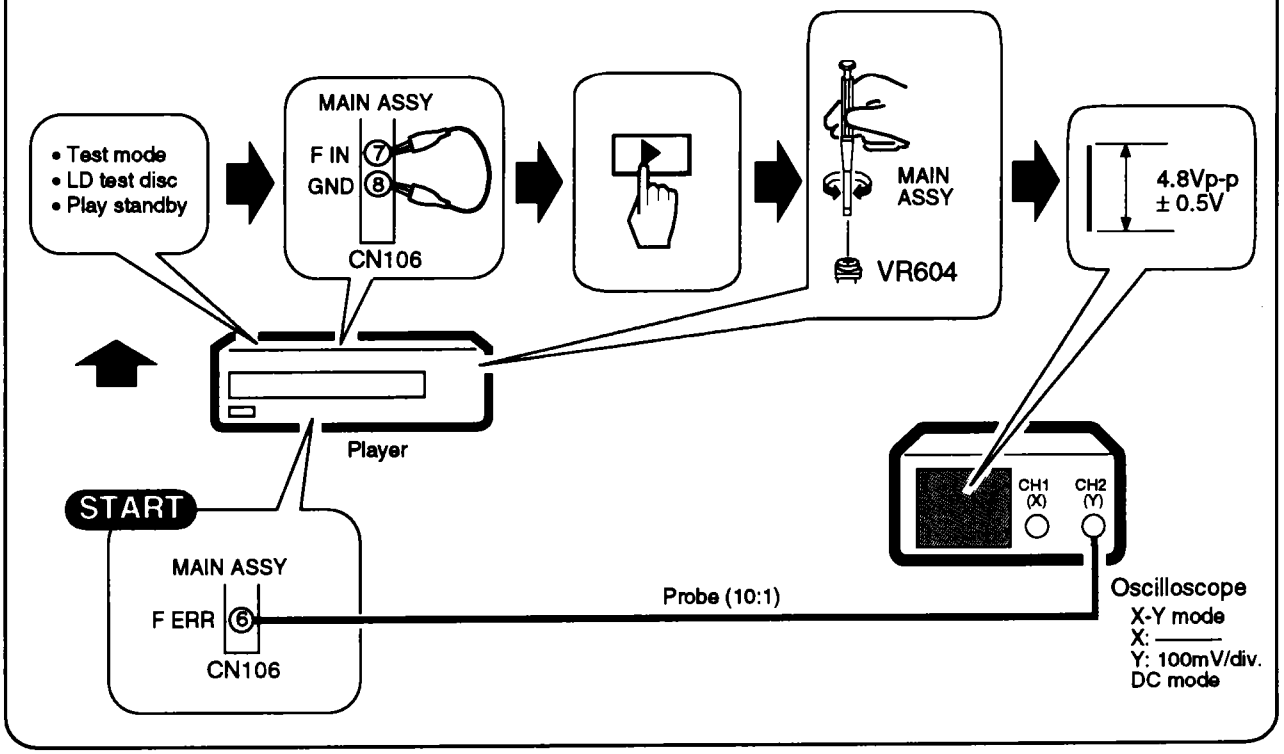


innermost : 最内周

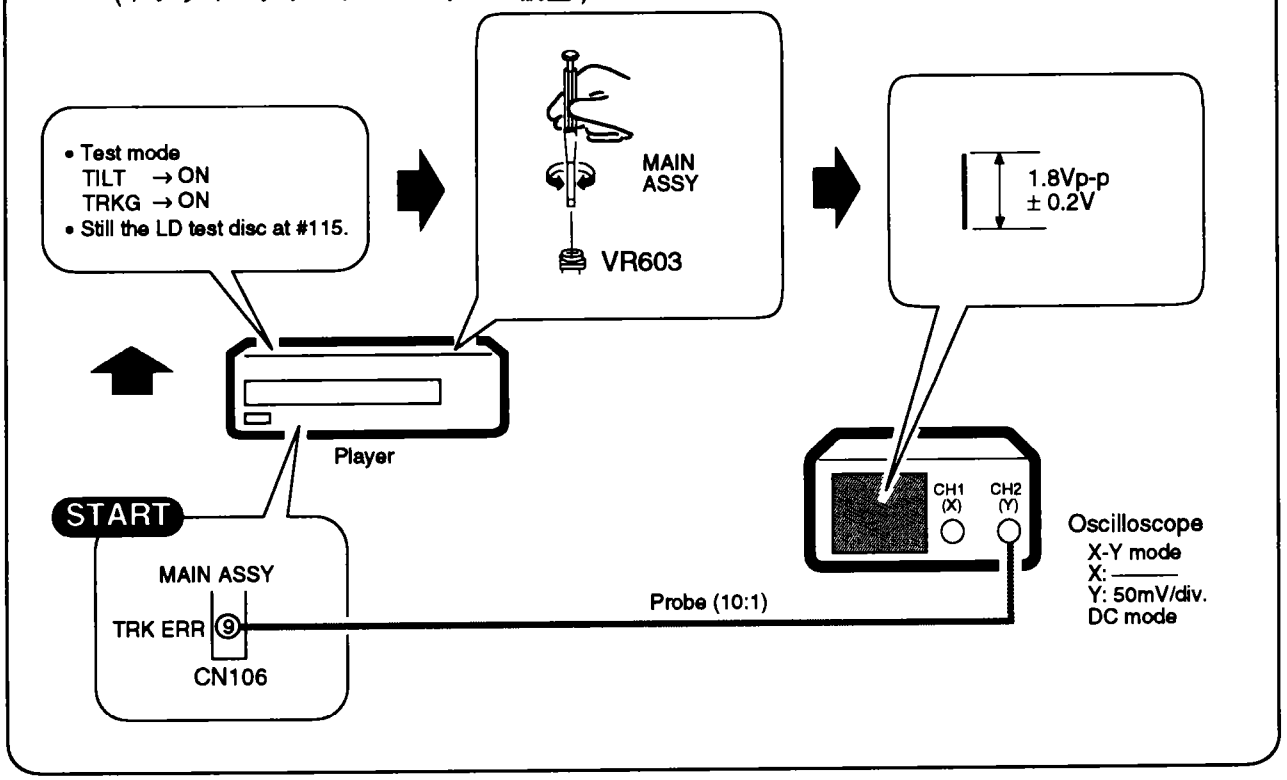
❹ Crosstalk Check and Fine Tilt Offset Adjustment for Side A
(A面クロストーク確認及び，チルトオフセット微調)



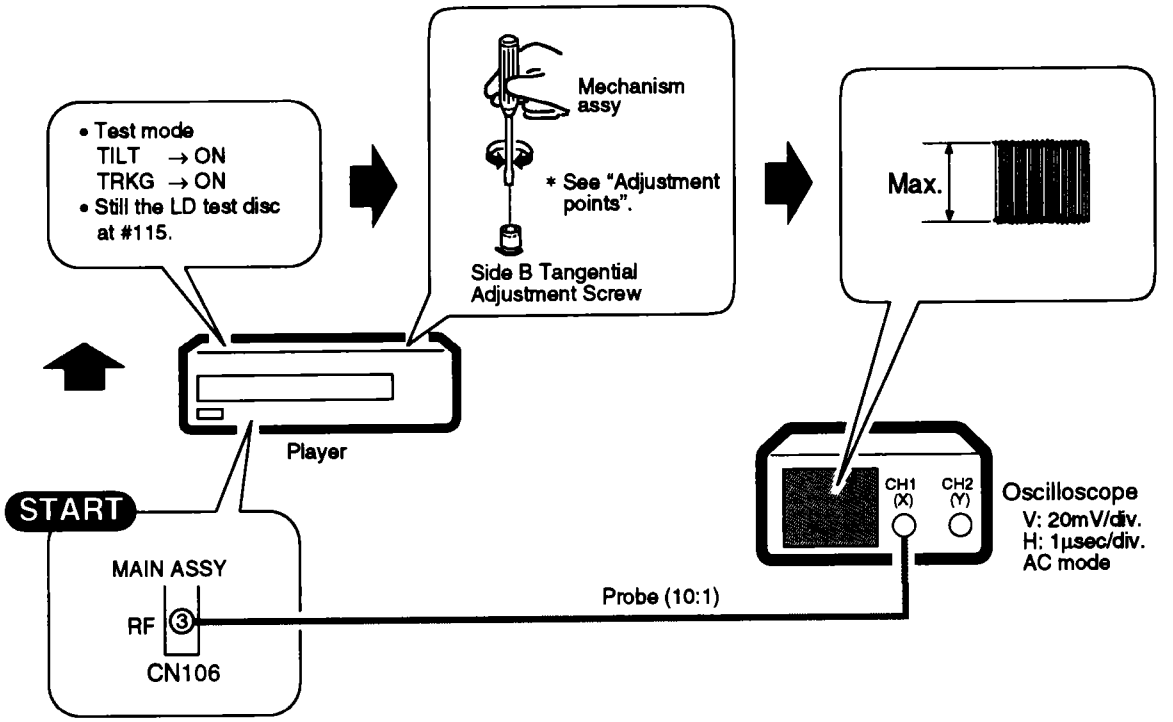
5 Focus Servo Loop Gain Adjustment
(フォーカスサーボループゲイン調整)



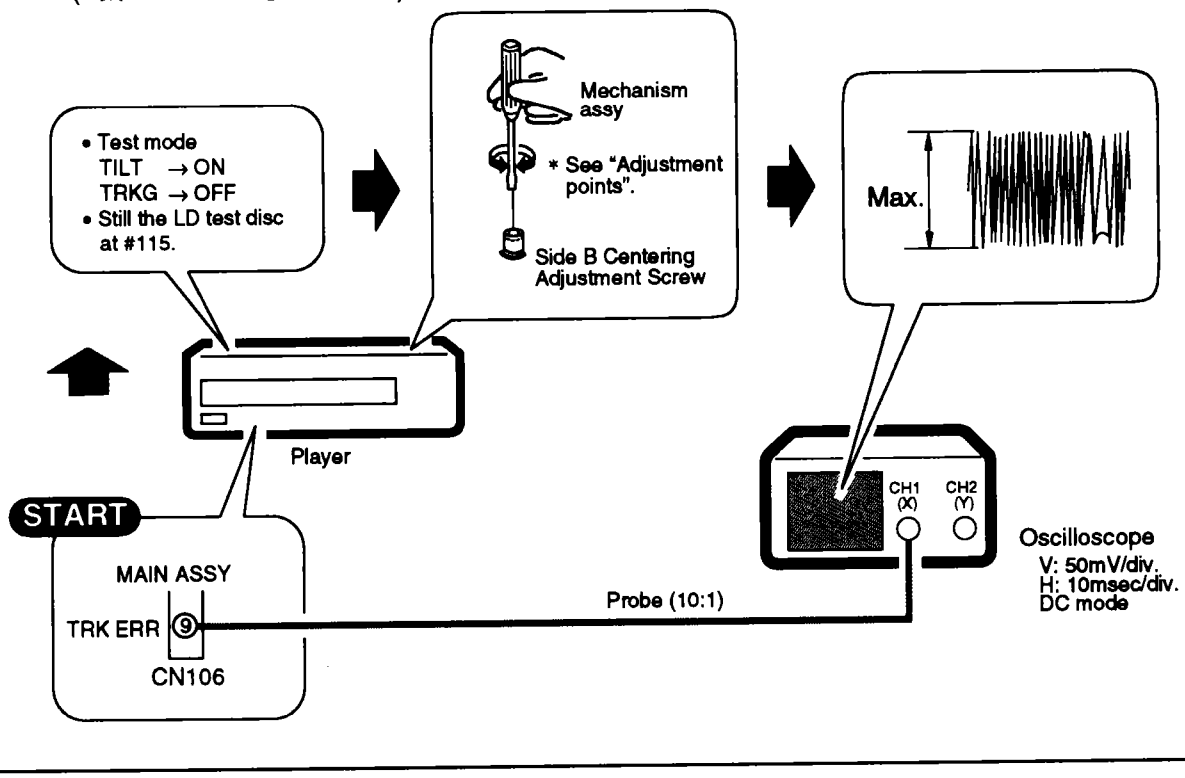
6 Tracking Servo Loop Gain Adjustment
(トラッキングサーボループゲイン調整)



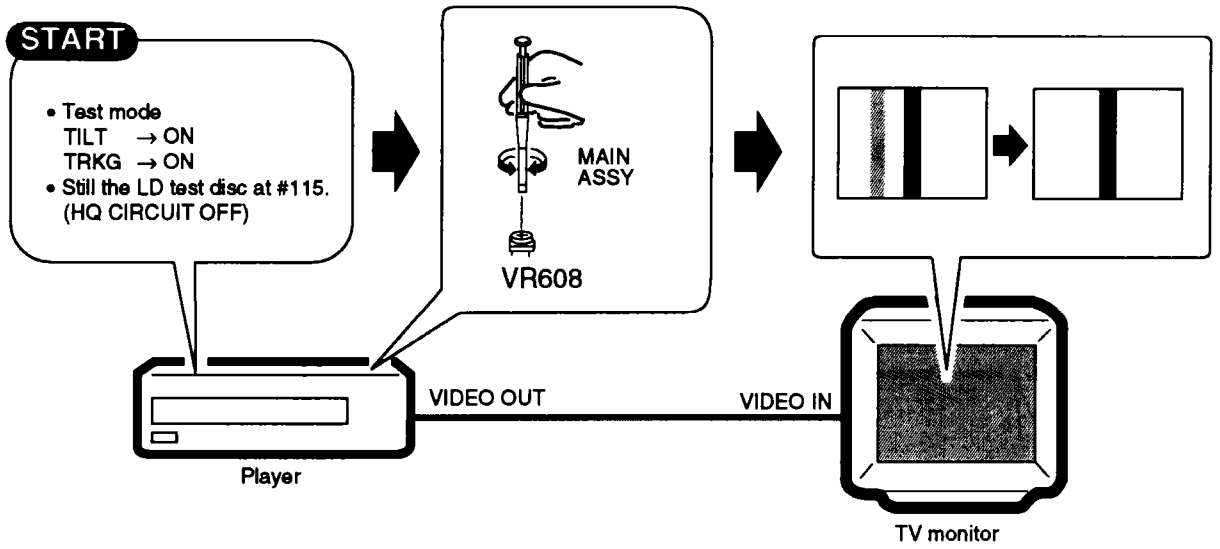
7 Tangential Direction Angle Adjustment for Side B
(B面タンジェンシャル傾き調整)



8 Spindle Motor Centering Adjustment for Side B
(B面スピンドル芯出し調整)

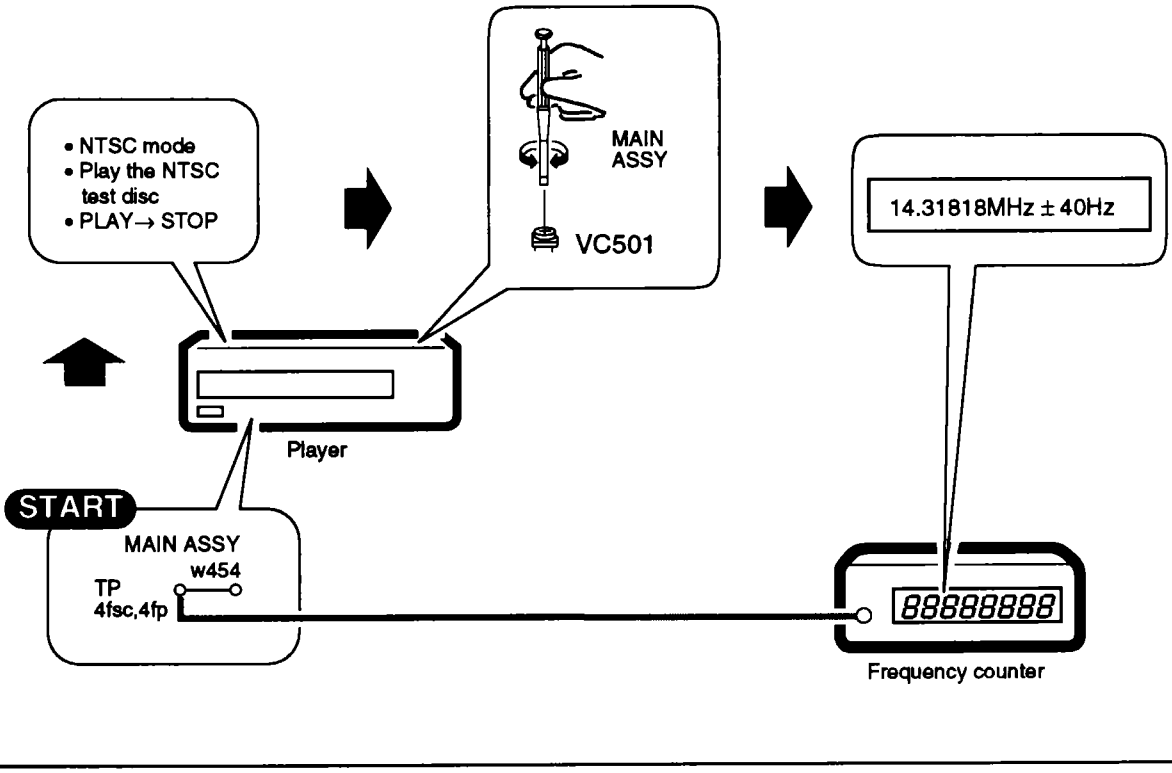


⑨ Crosstalk Check and Fine Tilt Offset Adjustment for Side B
(B面クロストーク確認及び，チルトオフセット微調)

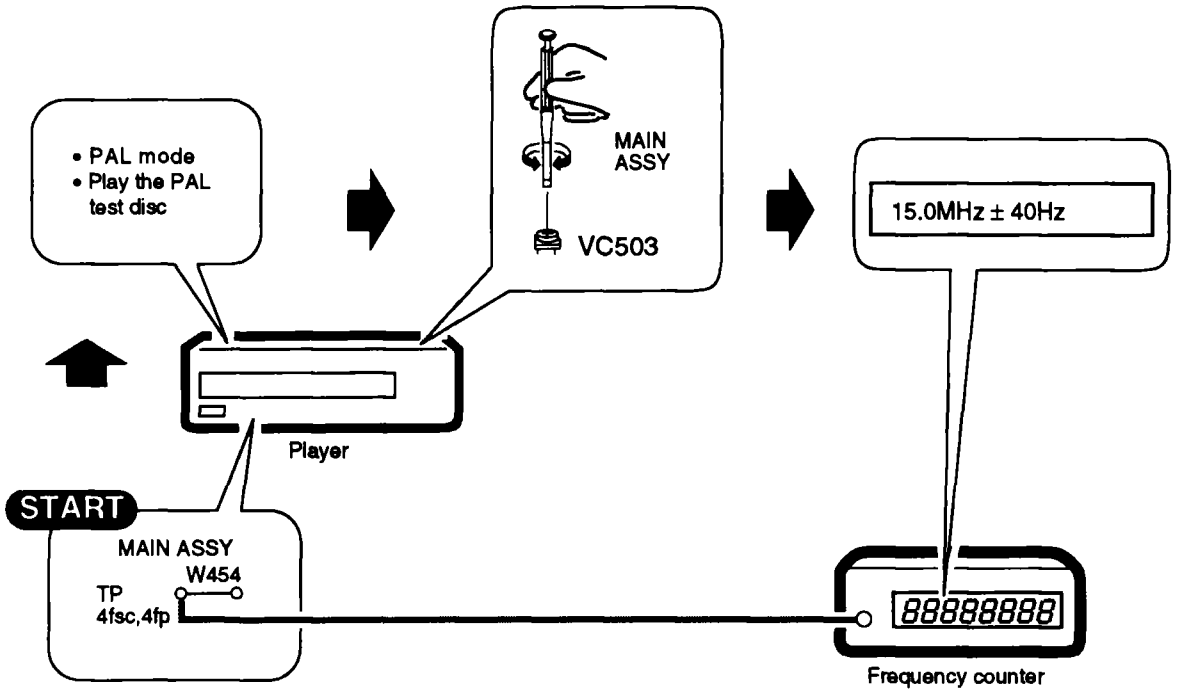


5.7 ELECTRICAL ADJUSTMENT of MAIN ASSY (MAIN ASSYの電気系調整)

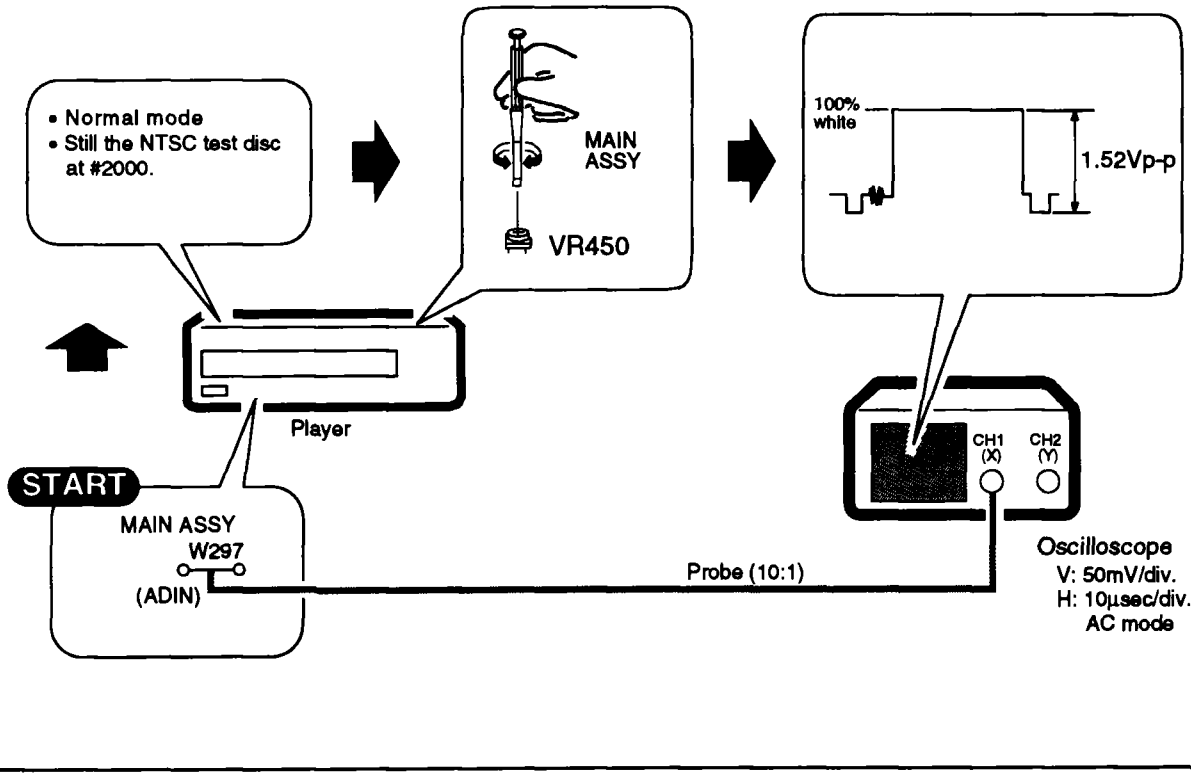
① NTSC Master Clock Adjustment
(NTSCマスタークロック調整)

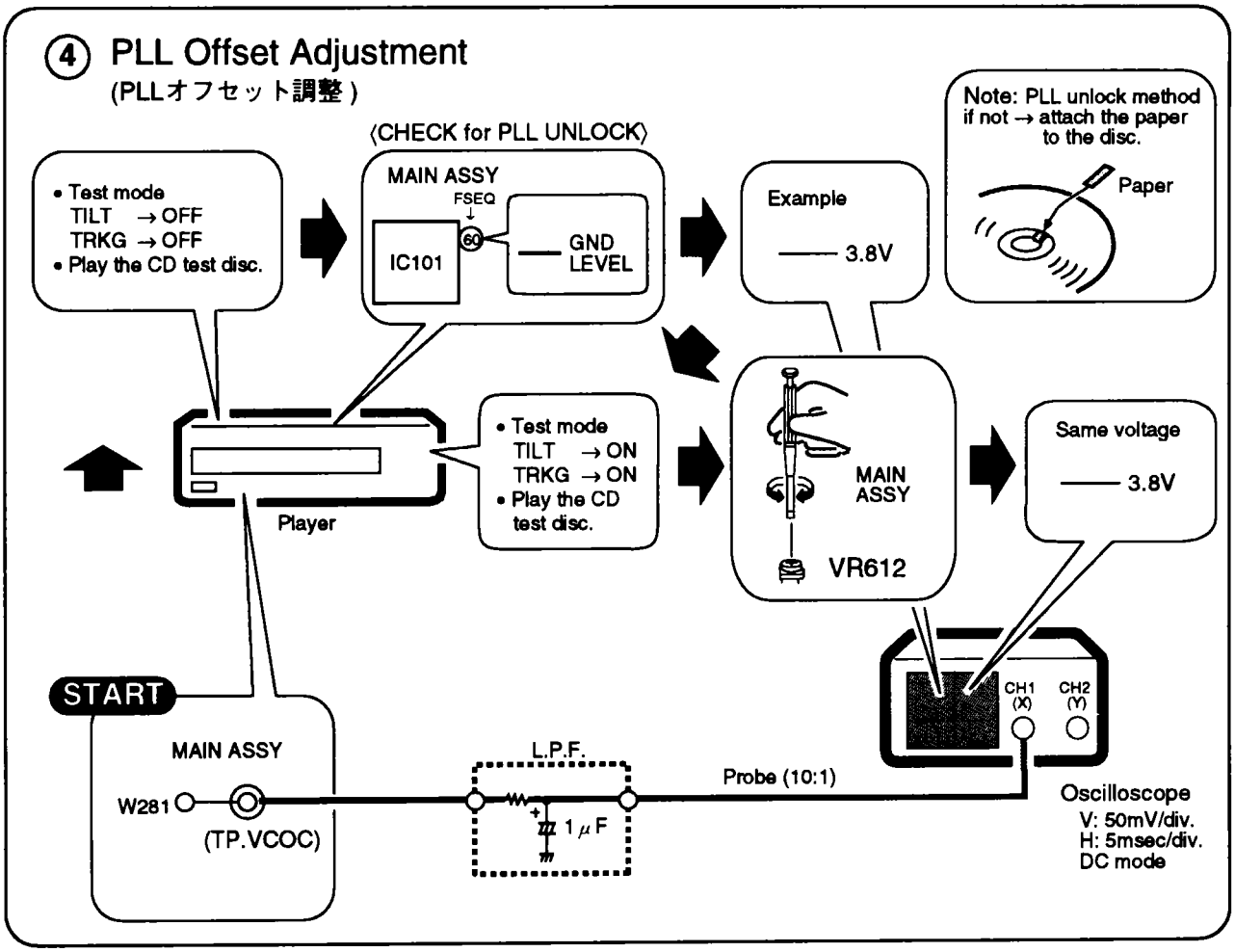


② PAL Master Clock Adjustment
(PALマスタークロック調整)



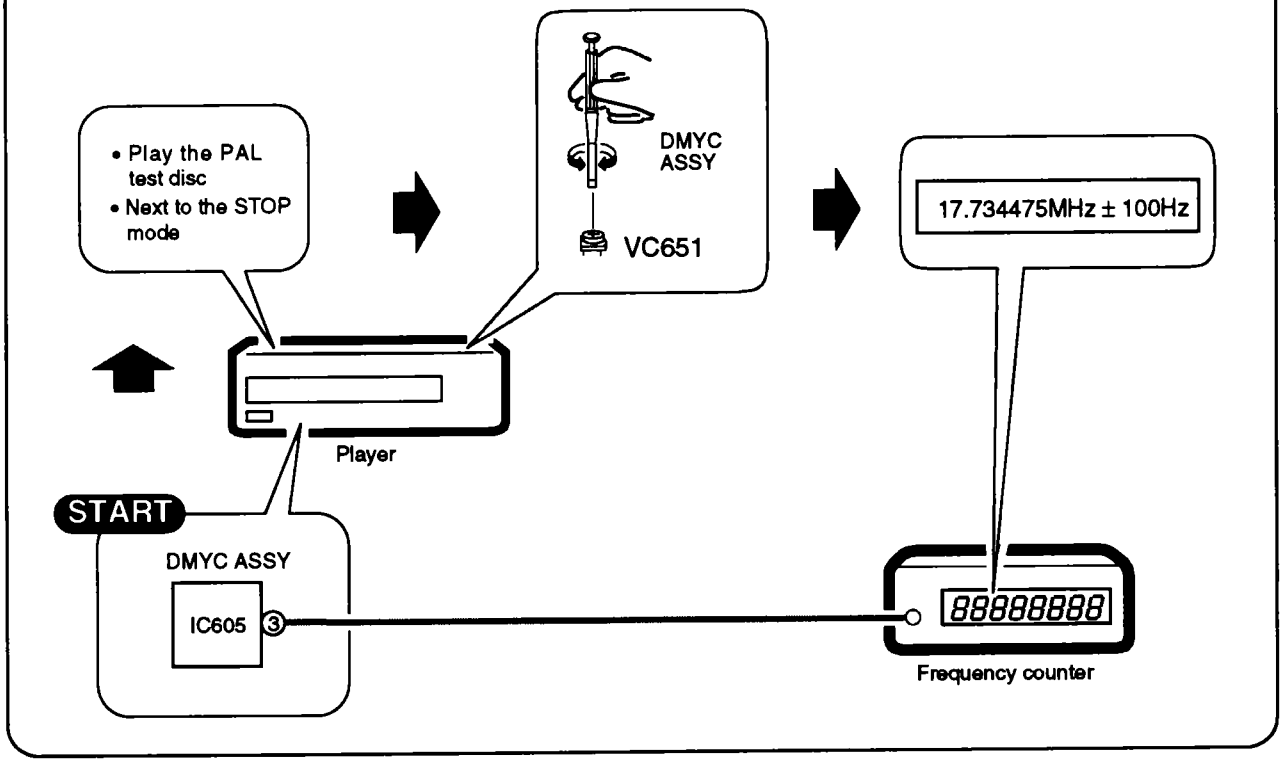
③ Output Video Level Adjustment
(出力ビデオレベル調整)



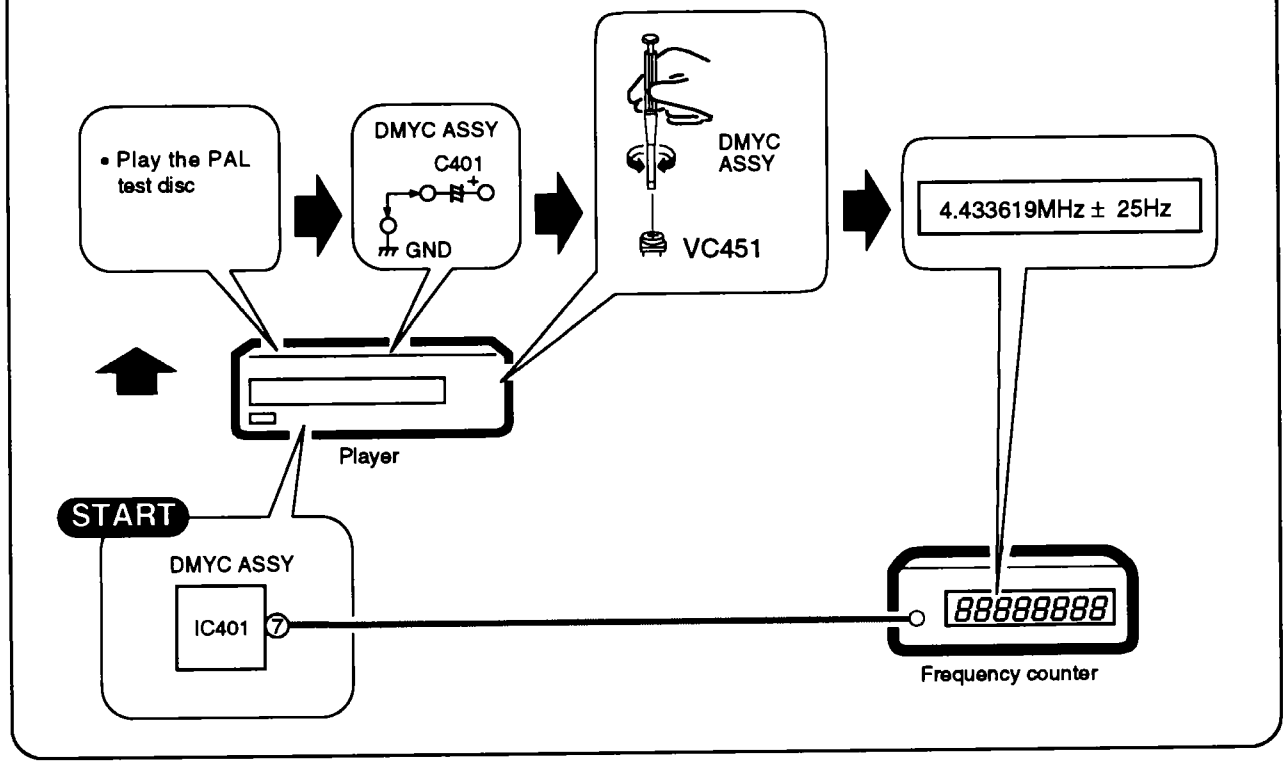

④ PLL Offset Adjustment
(PLLオフセット調整)
〈CHECK for PLL UNLOCK〉
• Test mode
TILT → OFF
TRKG → OFF
• Play the CD test disc.
MAIN ASSY
FSEQ
IC101
64
GND LEVEL
Example
3.8V
Note: PLL unlock method
if not → attach the paper
to the disc.
Paper
Player
• Test mode
TILT → ON
TRKG → ON
• Play the CD test disc.
MAIN ASSY
VR612
Same voltage
3.8V
START
MAIN ASSY
W281
(TP.VCOC)
L.P.F.
1 μF
Probe (10:1)
CH1 (X)
CH2 (Y)
Oscilloscope
V: 50mV/div.
H: 5msec/div.
DC mode

5.8 ELECTRICAL ADJUSTMENT of DMYC ASSY (DMYC ASSYの電気系調整)

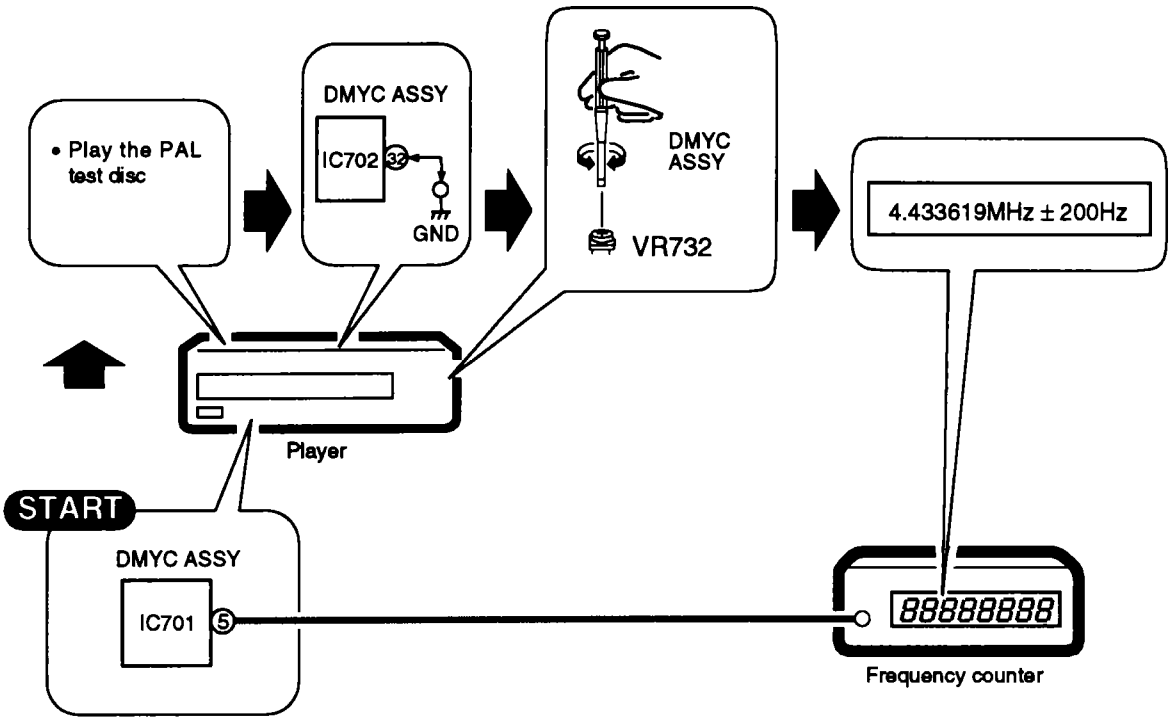
① 17MHz Free-run Frequency Adjustment
(17MHzフリーラン周波数調整)



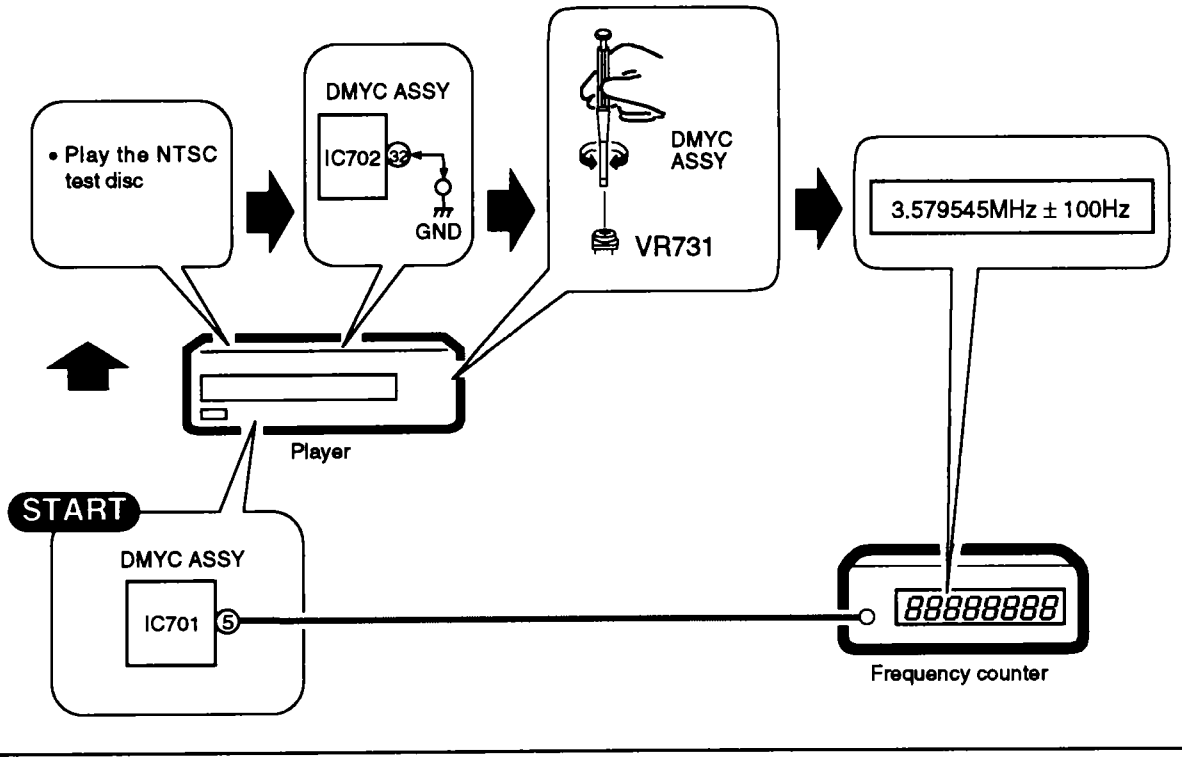
② 4.43MHz Free-run Frequency Adjustment for Y/C Separation
(Y/C分離用4.43MHzフリーラン周波数調整)



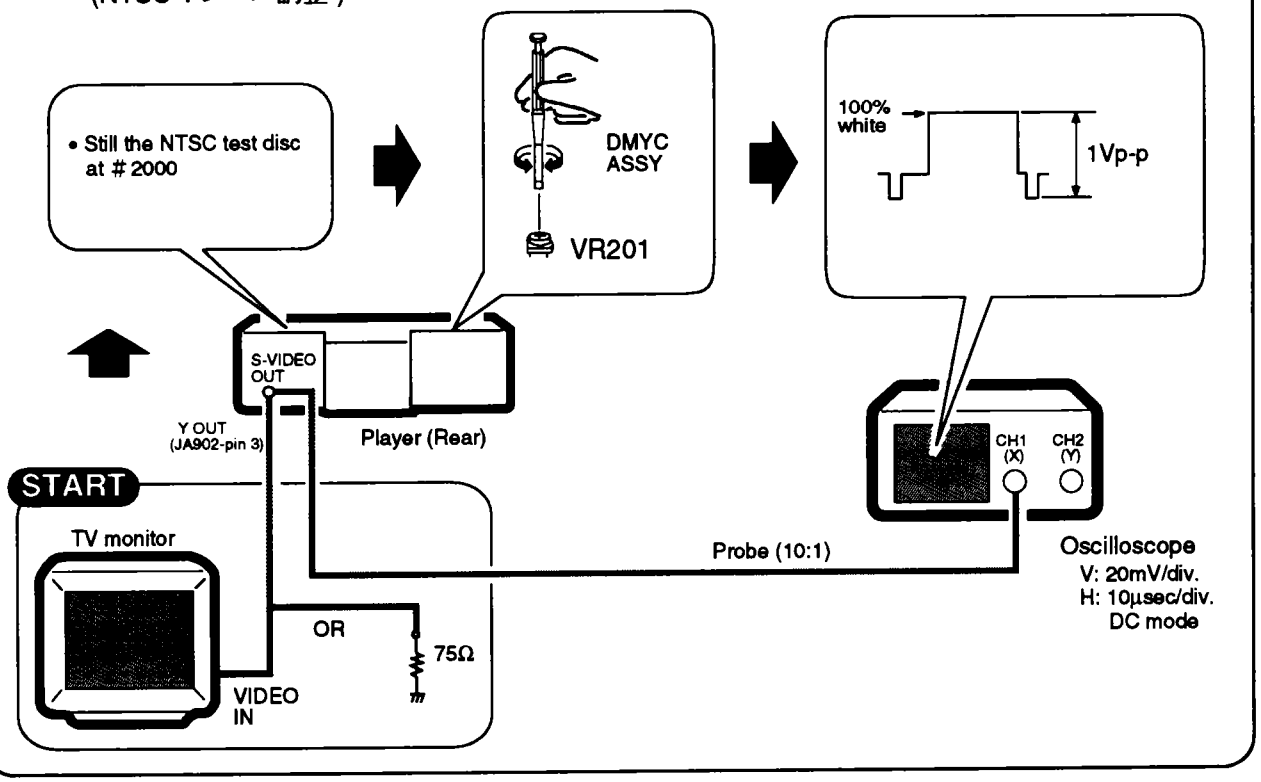
③ PAL 4.43MHz Free-run Frequency Adjustment for RGB Decoder
(RGBデコーダ用PAL 4.43MHz フリーラン周波数調整)



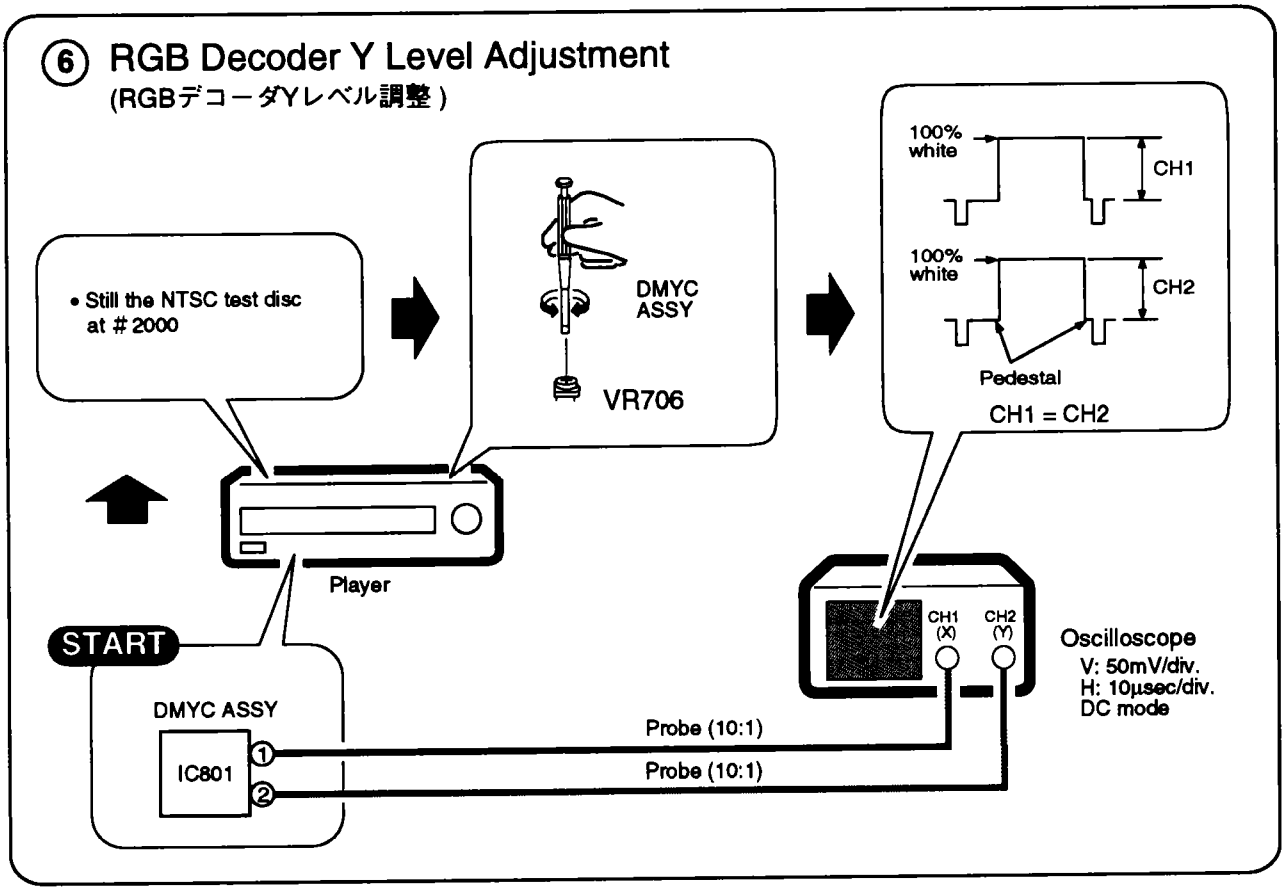
④ NTSC 3.58MHz Free-run Frequency Adjustment for RGB Decoder
(RGBデコーダ用NTSC 3.58MHz フリーラン周波数調整)



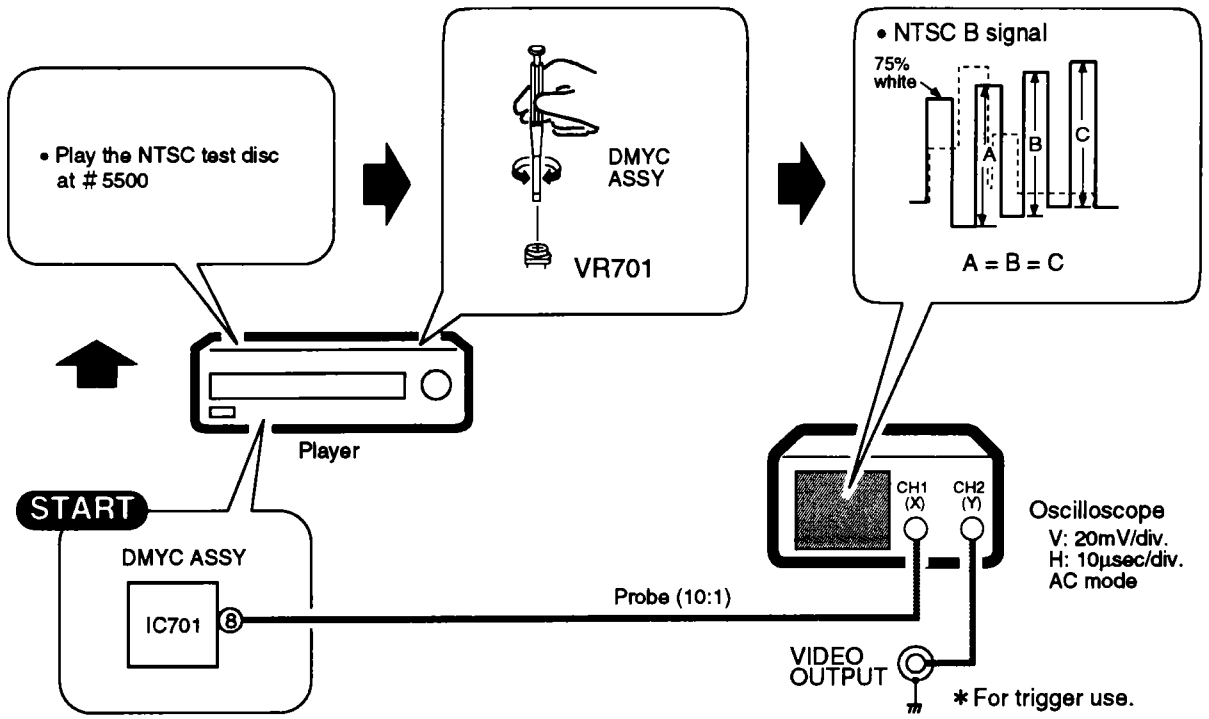
⑤ NTSC Y Level Adjustment
(NTSC Yレベル調整)



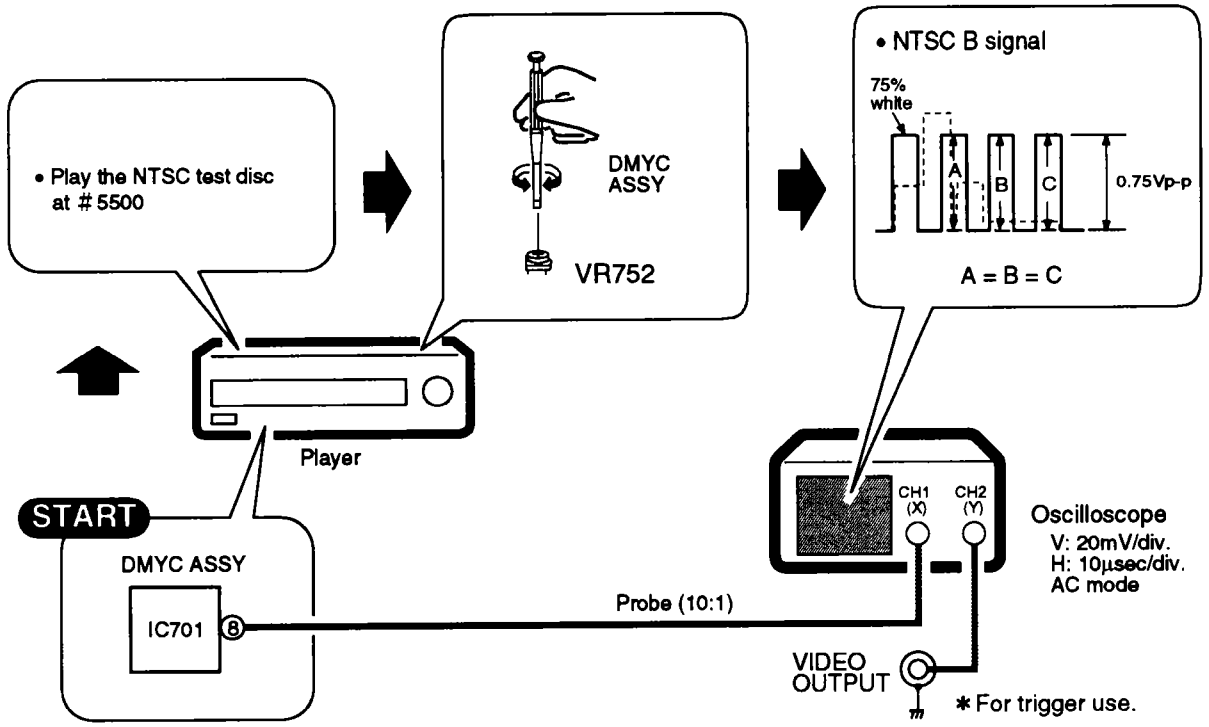
⑥ RGB Decoder Y Level Adjustment
(RGBデコーダYレベル調整)



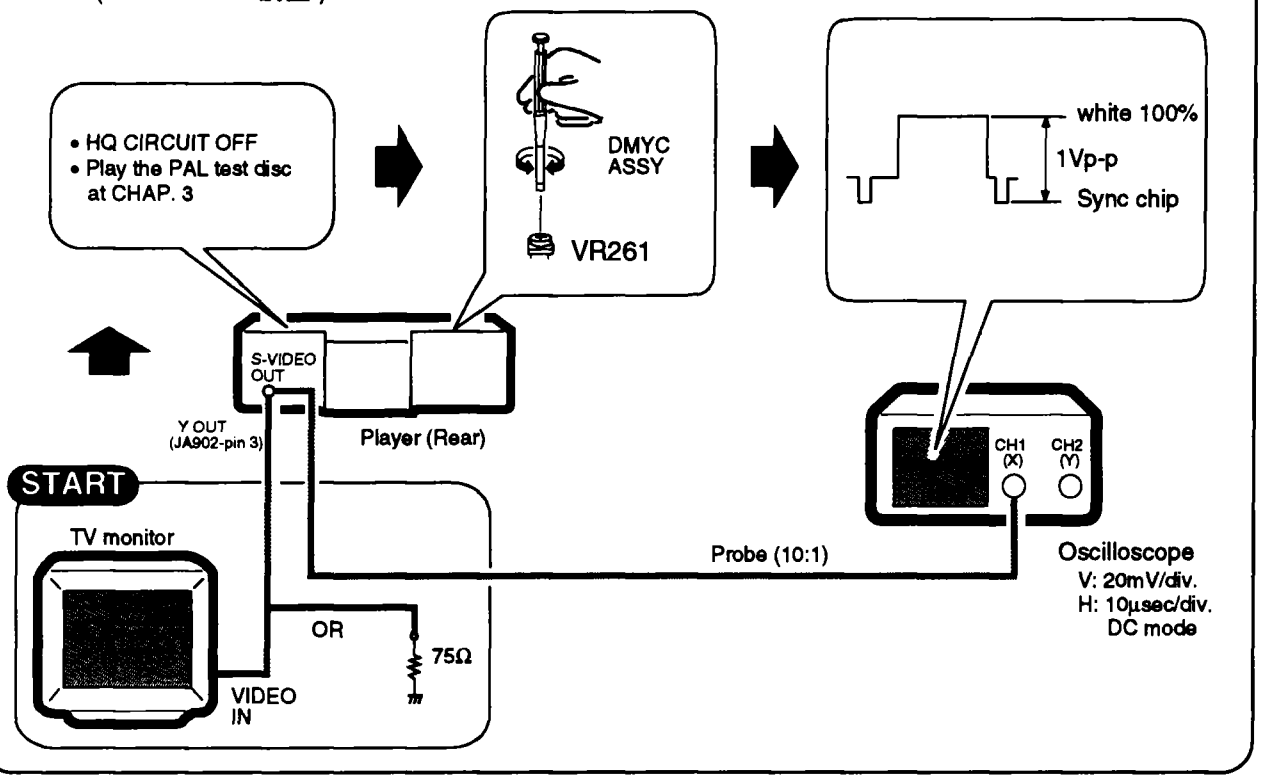
⑦ RGB Decoder HUE Adjustment
(RGBデコーダHUE調整)



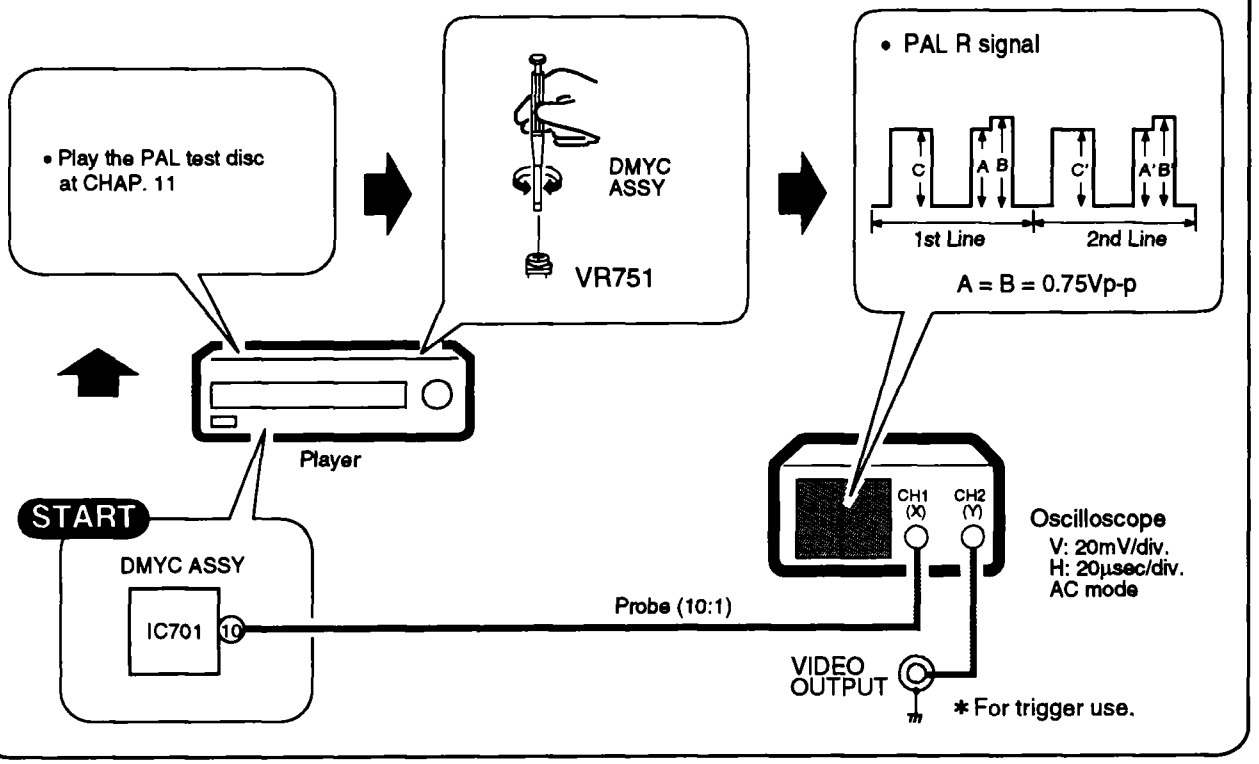
⑧ RGB Decoder NTSC Chroma Level Adjustment
(RGBデコーダNTSCクロマレベル調整)



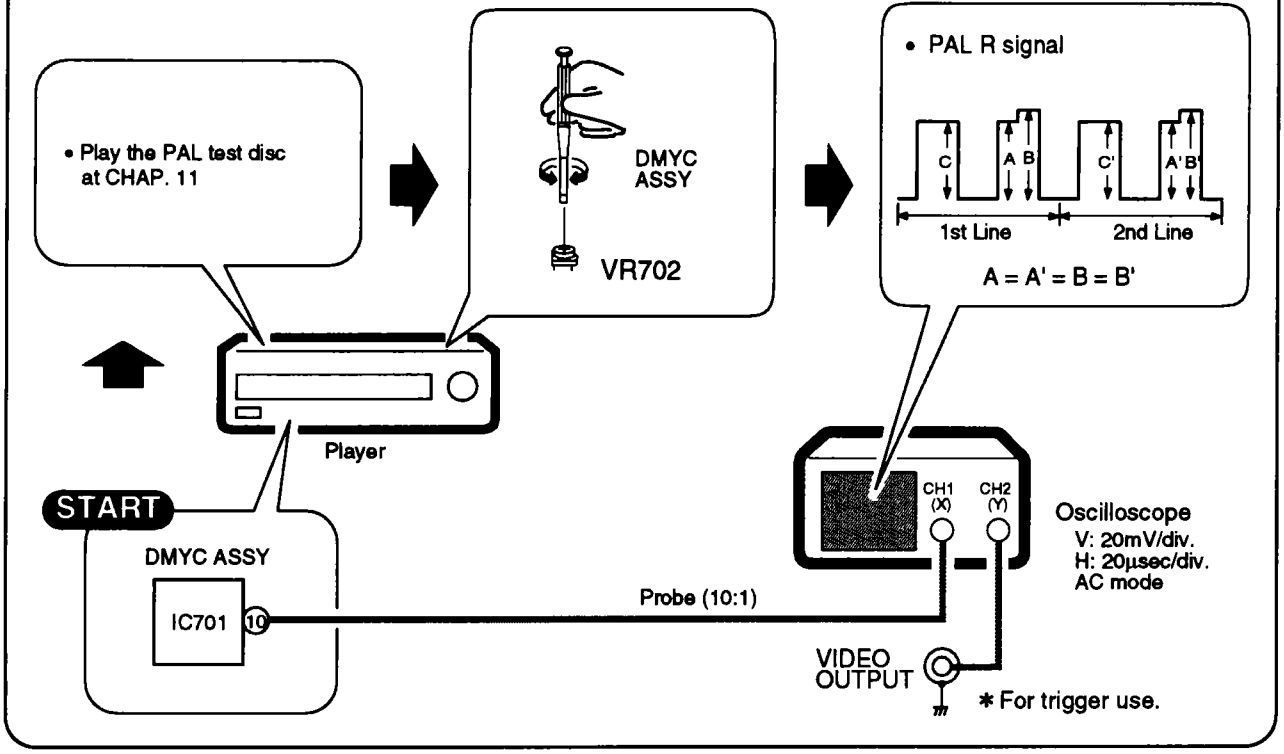
⑨ PAL Y Level Adjustment
(PAL Yレベル調整)



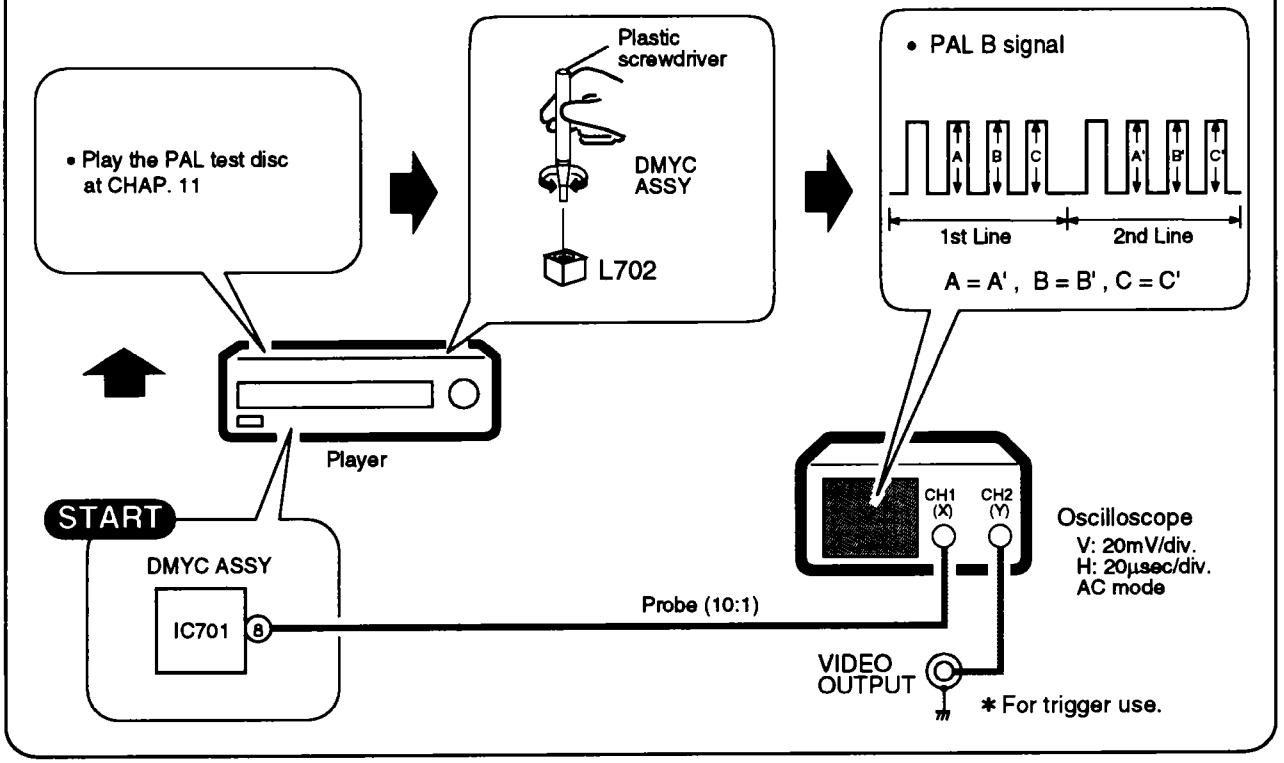
⑩ Coarse RGB Decoder PAL Chroma Level Adjustment
(RGBデコーダPALクロマレベル粗調整)



(11) RGB Decoder PAL Delay Line Amp. Gain Adjustment
(RGBデコーダPALディレーラインアンプゲイン調整)

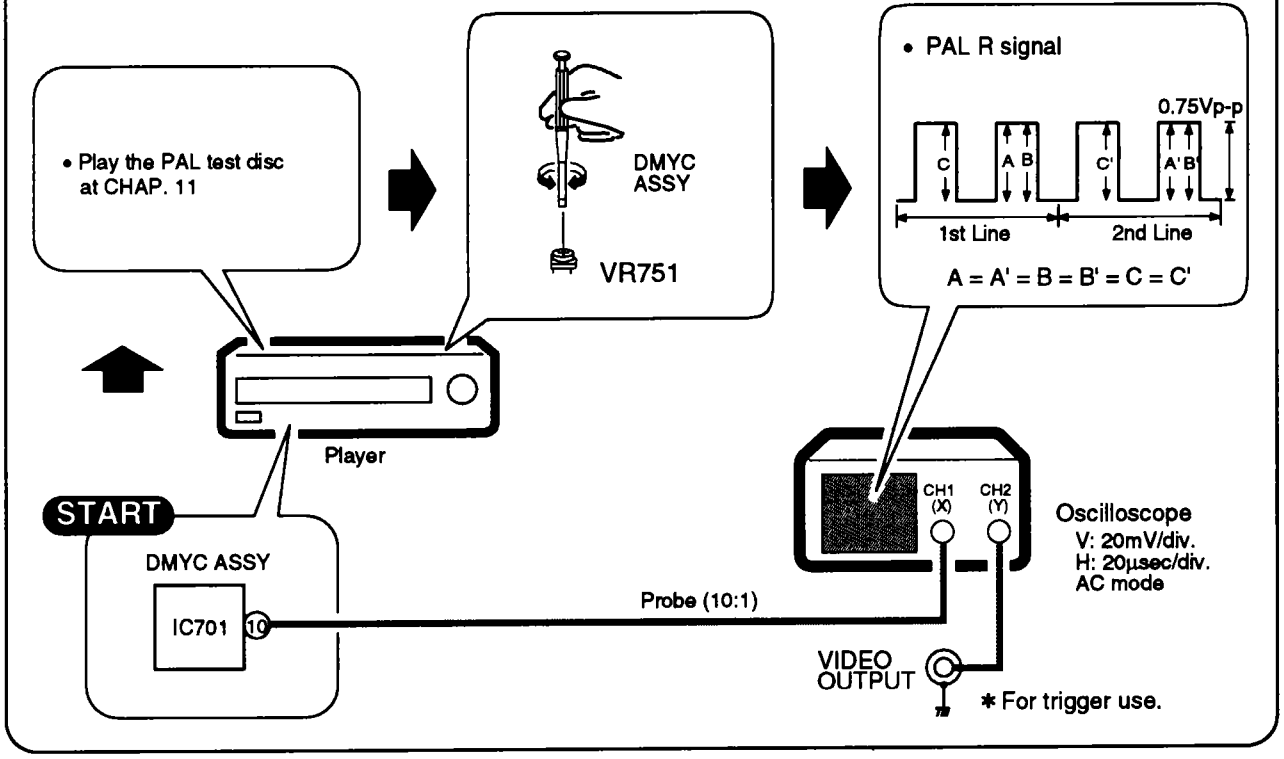


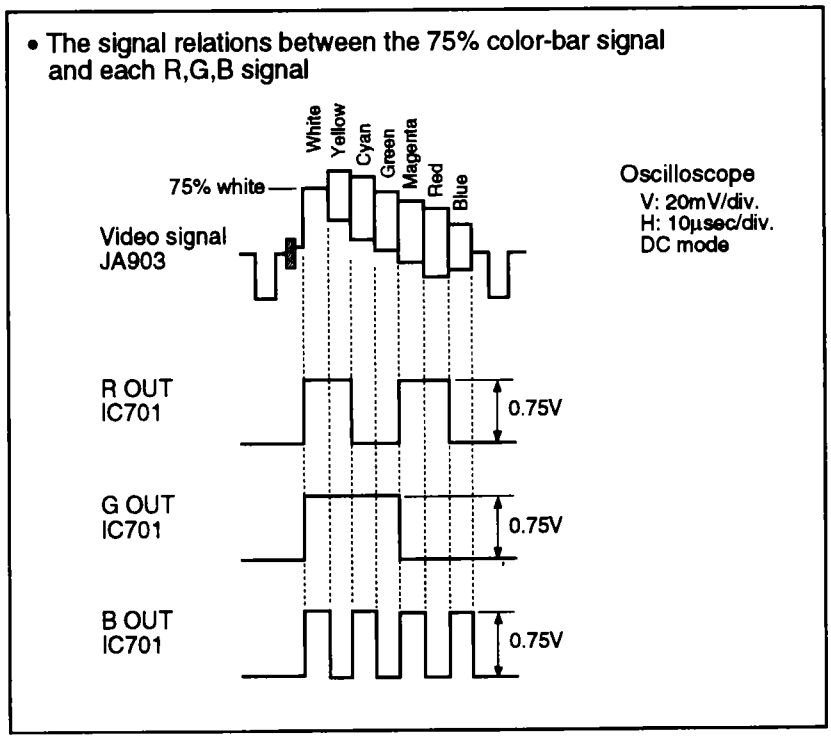
(12) RGB Decoder PAL DAT Adjustment
(RGBデコーダPAL DAT調整)



⑬ Fine RGB Decoder PAL Chroma Level Adjustment

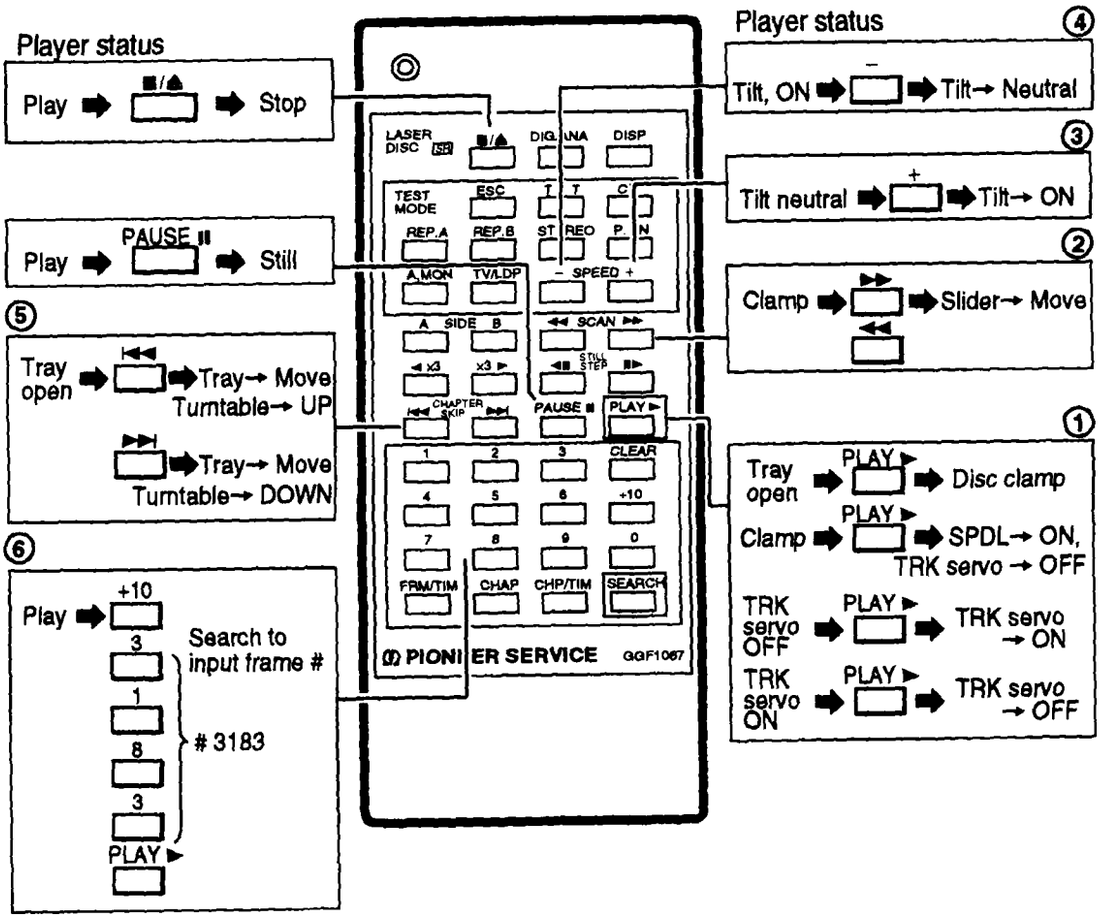
(RGBデコーダPALクロマレベル微調整)



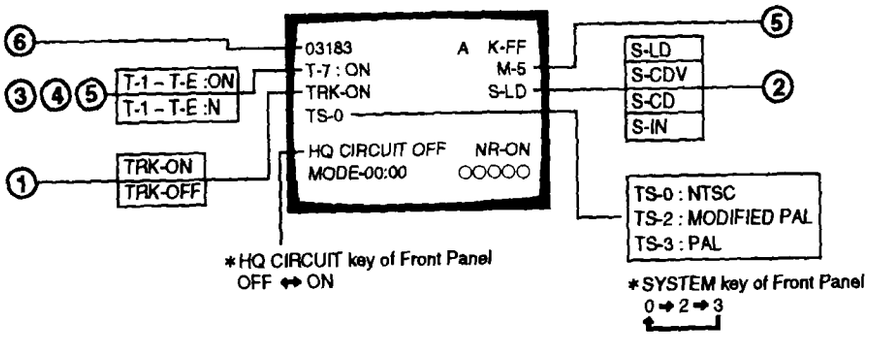


5.9 OPERATIONS IN THE TEST MODE (テストモード時のサービス用リモコン操作方法)

■ Test Mode Remote Control Unit (GGF1067)



■ TV Monitor Display



6. SELF-DIAGNOSTIC FUNCTIONS

6.1 SELF-DIAGNOSTIC FUNCTIONS

The self-diagnostic functions automatically display an error code on the TV screen and front panel fluorescent display section when there is an error. The customer checks the error code and conveys it to the service personnel to make repairs more efficient.

After an error occurs, even if the error code goes off, you can display the error code again by holding down the [CLEAR] key for 5 seconds (except a loading error [L *] display). At that time, partial error is displayed with the mechanism switch information.

* : If the Power Cord is unplugged, this function is not lost with the EEPROM IC (IC102).

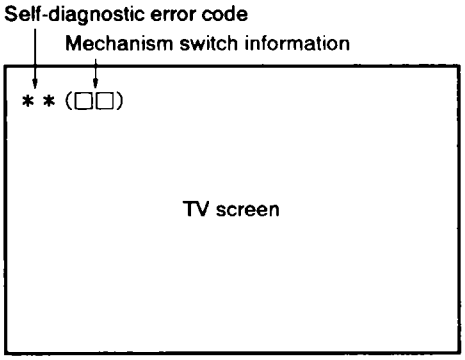


Fig. 1 TV screen display

This table explains the information for analyzing the cause when an error occurs with the CLD player.

Self-diagnostic error code	Contents	Conditions	Probable cause
H0	Spindle overcurrent detection error.	In the play state, overcurrent was detected in the spindle motor. Monitoring starts 5 seconds after the start of play or special playback mode, this error is detected if the overcurrent port is "L" for 4 seconds.	• Motor NG • Clamper rubbing
U0	FG abnormality error	① At LD start-up, the rate of rotation calculated from the FG was less than 15 rpm for 5 consecutive seconds from the spindle run command. ② At CD start-up, there was less than 1/8th rotation even after 5 seconds had passed since the end of acceleration. ③ During play search, CD : subcordes are being read/LD : Phillips codes are being read and the spindle is locked, but a state in which the rate of rotation calculated from the FG was less than 15 rpm continued for 5 seconds or more. In the above case, it is judged that an abnormality has occurred in the FG sensor and that accurate rotation rate calculation has become impossible.	• FG sensor abnormality, FG signal not coming to mechanism controller • FG sensor clogged • Rubbing between FG sensor and slit • Turntable dropped • FG slit deposition NG
H1	Partial short error	① At LD start-up, the speed did not reach 1200 rpm within a certain time (12 seconds) after the spindle run command. ② At CD start-up, a certain speed (313 rpm) was not reached within 6 seconds from the end of spindle acceleration.	• Spindle motor NG • Commutator NG • Bearing too tight • Power supply NG
H2 A0	Power supply abnormality error	− 5V power supply abnormality detected. The power supply abnormality port is constantly monitored and if its signal stays high for about 1 second consecutively, the power supply is judged to be abnormal.	• − 5V not fed from POWER SUPPLY assy • Parts shorted
L *	Loading error	① When loading operation goes over time (approx. 10 sec.). ② When assist at disc sense entry ends and is not tilt neutral. ③ When assist at set up entry ends and is not tilt neutral.	• Tilt switch 1, 2, 3 abnormal, so tilt/loading state not read in correctly • Tilt/loading mechanism mechanically locked • Drive IC NG • Power supply NG
E *	Slider error	During slider movement, a time over-run occurred (track count search 20 seconds, mandatory movement 10 seconds)	• Slider ceased being able to run • The slider mechanism is mechanically locked and can no longer move to its target. • Slider position switch NG • Flexible cable pulled out • Drive IC NG • Power supply abnormal
U1	Miss clamp error	① During LD setup, after 1/8th rotation, the track count during 1/8 rotation exeeded 511. ② During start-up, the focus was lost once and refocusting was attempted, but the focus could not be locked. ③ Two FG pulses did not come within 800 ms from from the start of LD start-up. ④ The disc clamp operation did not end within 5 seconds.	• Disc sandwiched • Disc shifted • Spindle motor NG • Disc scratched or dirty defocused during start-up • Two discs loaded • PU actuator NG • Tilt sensor NG • Tilt neutral NG (tilt base NG)

Self-diagnostic error code	Contents	Conditions	Probable cause
P ＊	Spindle error	①During TOC reading with an LD, the spindle servo was not locked within 60 seconds from the start of the spindle run. ②When CAV/CLV determination is not finished within 60 seconds from spindle servo lock. ③The codes could not be read for 10 – 15 seconds consecutively for an LD or 7 – 10 seconds for a CD/CDV and the spindle servo was not locked. ④The speed exceeded 2100 rpm during LD start up.	P0 :•PH code, SUB-Q code can not be read •VCO, PLL offset out of adjustment •Disc defect P5:•PAL disc, mirror disc, etc. PLAY •No RF P6:•Spindle servo does not lock •Spindle motor NG
F ＊	Focus error	①"In the "no disc" state, a setup command was received from the mode controller. ②When LD is out of focus when slider is moved to starting position during set up. In case of CD/CDV is NG even after three focus tries. ③During start-up, the maximum slider servo duty continued for 3 loops or more.	F5 :•CD, LD on top of each other •LD scratched or dirty defocused during slider movement •Disc NG •Slider position switch NG F6 :•Inner edge of disc scratched or dirty •Slider ran into inner edge mechanical stopper

＊ Besides the above errors, there is the "U2" communications error (the mode controller could not communicate normally with the mechanism controller)
The probable cause is a defective mechanism controller, disconnected cable, etc..
＊ Mechanism mode contents (meanig of ＊ for L ＊ etc.)

0 : Play
1 : Open
2 : Standby
3 : Clamp
4 : Disc sense
5 : Setup (rotation start)
6 : TOC read
7 : Play
8 : Search
9 : Side A → Side B
A : Side B → Side A

6.2 FORMAT OF THE MECHANISM SWITCH INFORMATION WHICH IS TRANSMITTED TO THE MODE CONTROL IN THE ERROR OCCURRENCE

Hexadecimal number system	Binary number system
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
A	1 0 1 0
B	1 0 1 1
C	1 1 0 0
D	1 1 0 1
E	1 1 1 0
F	1 1 1 1

• Mechanism switch information (Example [1][7] **)**

Mechanism control → Mode control
Communication byte address 5 (COMBUF5)
(Mode control displays this value as it is.)

Hexadecimal number system

Example

Example

Hexadecimal number system [1]

Example [7]

Binary number system

0	0	0	1	0	1	1	1
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
TURN A	O Not used	LTSW1	LTSW2	LTSW3	SLDP1	SLDP2	SLDP3

TURNA	Slider position
0	Side B
1	Side A

LTSW 1	2	3	Loading/tilt position
0	1	1	Open (Tray open state)
0	0	1	Loading (During move the tray horizontally)
1	0	1	Standby (Tray close & spindle down state)
1	0	0	Clamp (Durring spindle up or down)
0	0	0	Tilt – (Clamp state)
0	1	0	Tilt + (Clamp state)
1	1	0	Tilt limit (Clamp state)

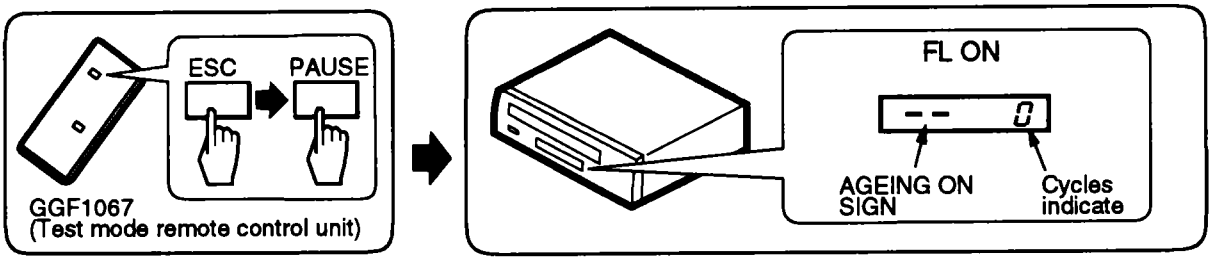
SLDP 1	2	3	Slider position
1	0	0	CD active position
1	0	1	CDV active position
1	1	0	LD active position
0	1	1	CD inside position
1	1	1	Side B inside position

Example of [1][7] is indicated as follows.

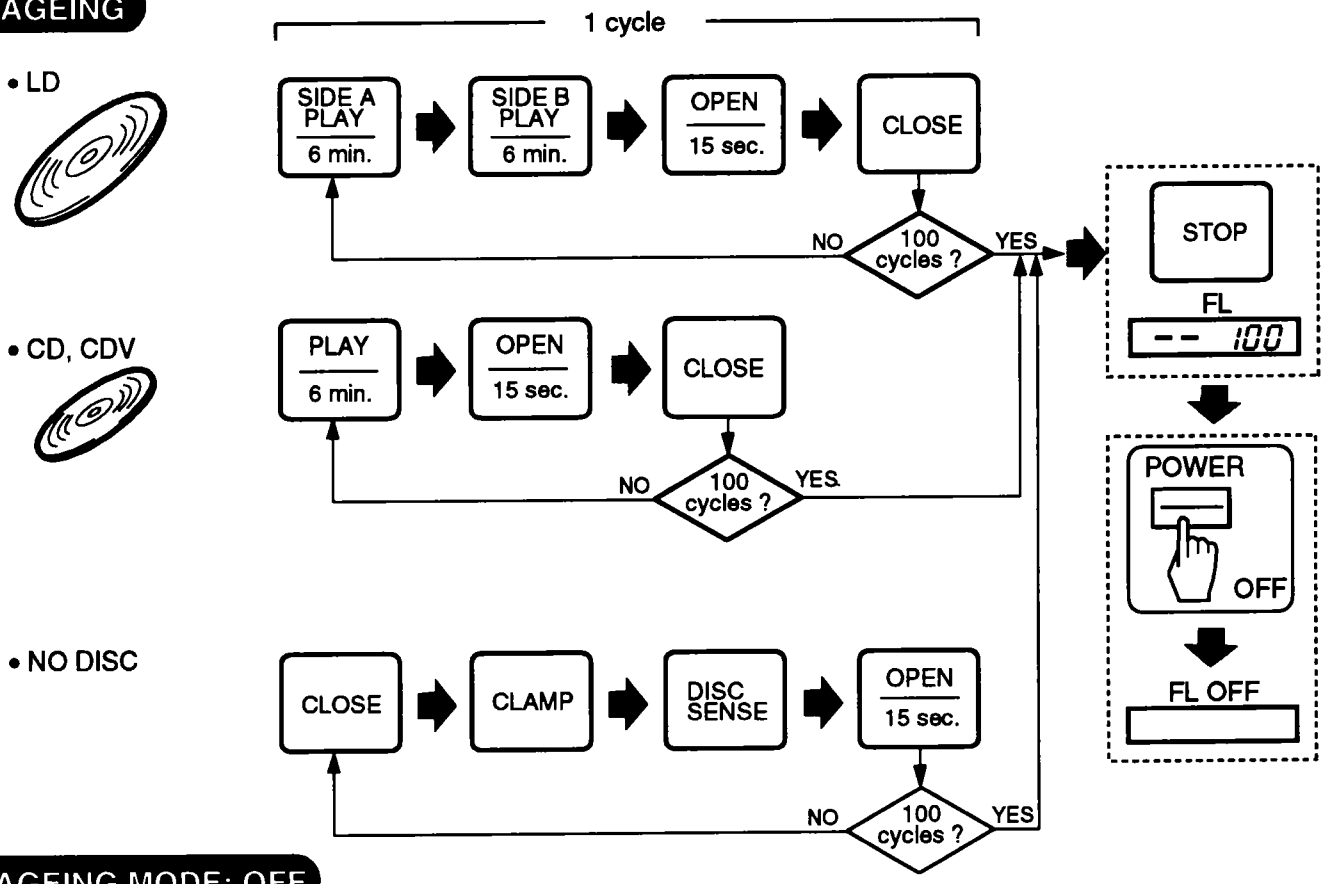
Slider : Side B
Tilt : Tilt +
Position : B-INSIDE

7. AGEING MODE (エージングモード)

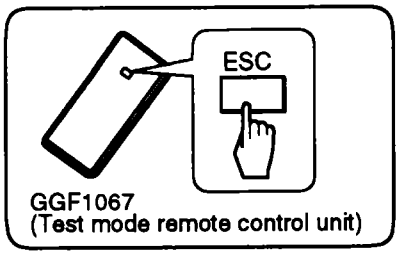
AGEING MODE: ON •Note for KARAOKE model : Set the SINGLE PLAY (一曲停止) mode to OFF.



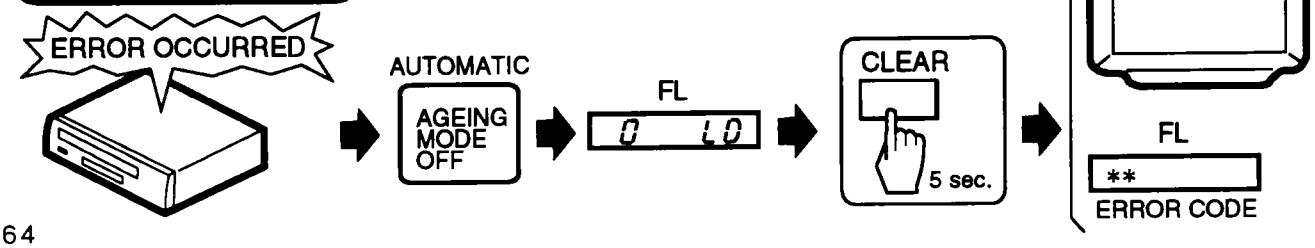
AGEING



AGEING MODE: OFF



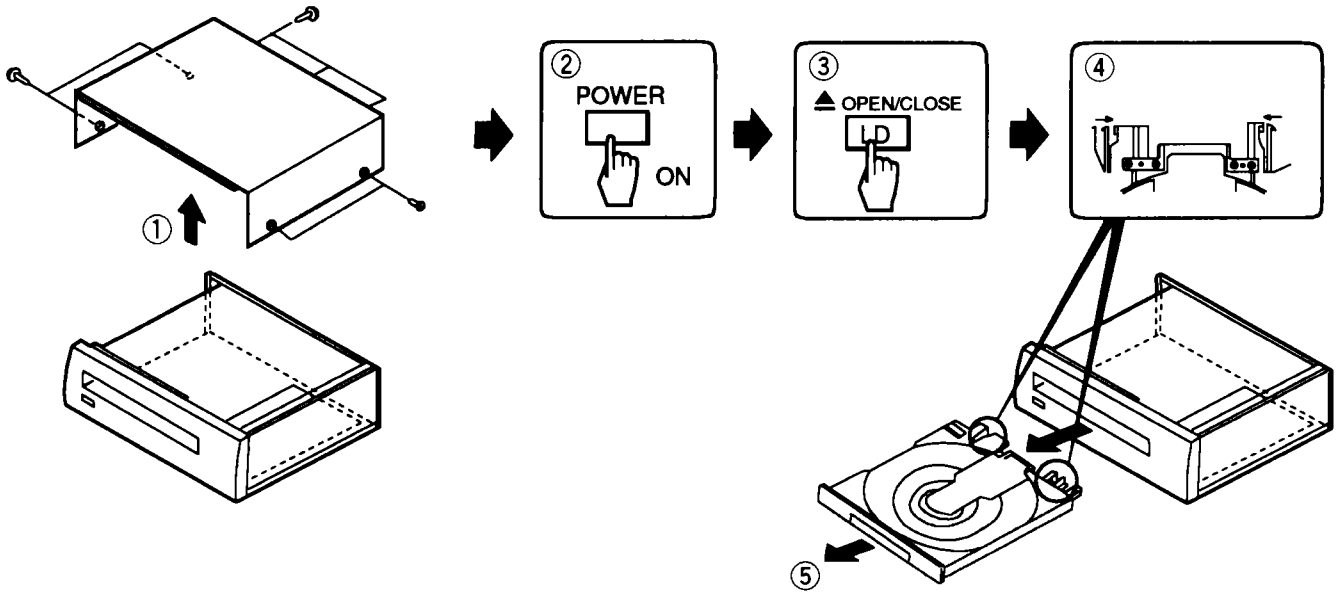
ERROR OCCURRED ERROR OCCURED : エラー発生



8. DISASSEMBLY/ASSEMBLY (分解/組立の手順)

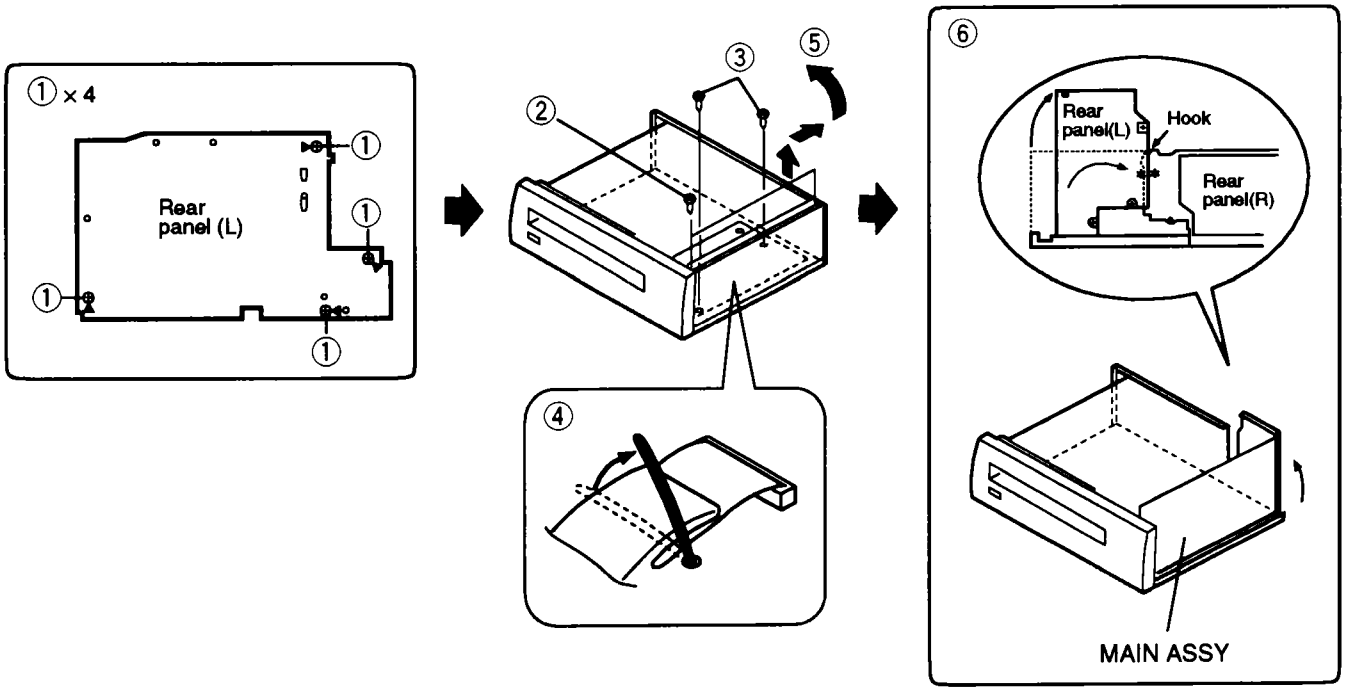
8.1 DISC TRAY

- Disassembly : ①→②→③→④→⑤
- Assembly : ⑤→①



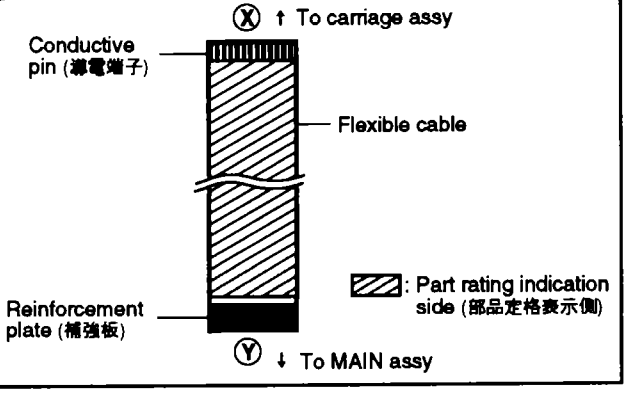
8.2 MAIN ASSY

- Disassembly : ①→②→③→④→⑤→⑥
- Assembly : ⑥→⑤→④→③→②→①

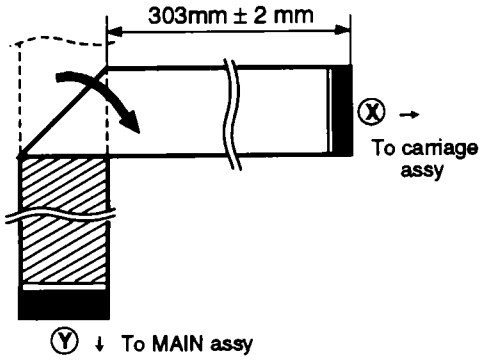


8.3 HOW TO INSTALL THE FLEXIBLE CABLE FOR CARRIAGE ASSY
(キャリッジASSY用フレキシブルケーブルの取付方法)

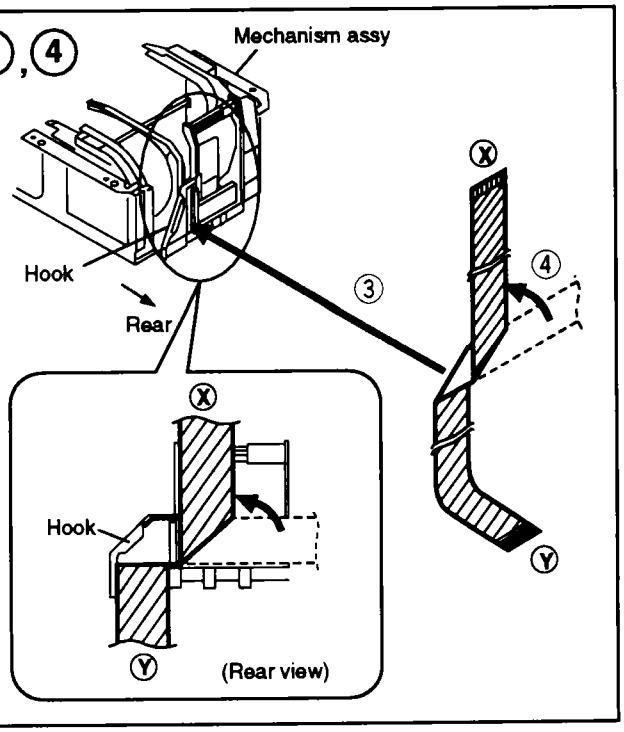
① New Flexible cable


Ⓧ ↑ To carriage assy
Conductive pin (導電端子)
Flexible cable
: Part rating indication side (部品定格表示側)
Reinforcement plate (補強板)
Ⓨ ↓ To MAIN assy

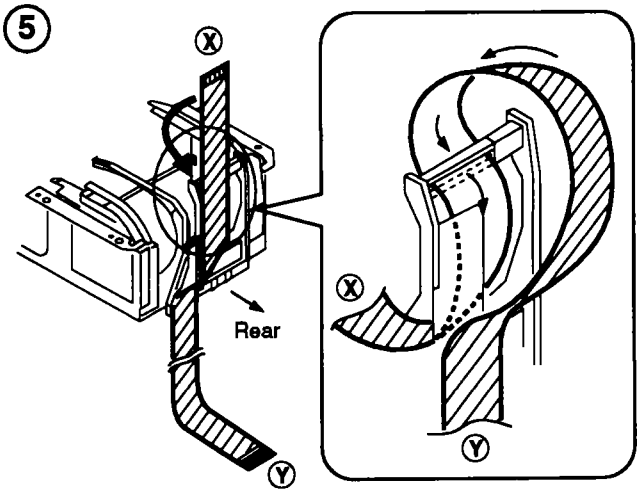
② Bend the Flexible cable
(フレキシブルケーブルを折り曲げる)



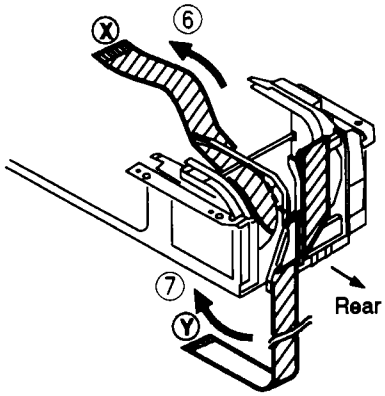
③, ④



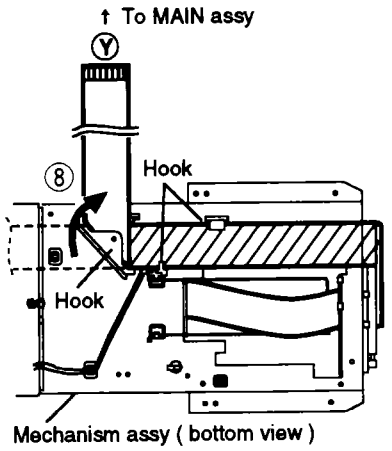
⑤

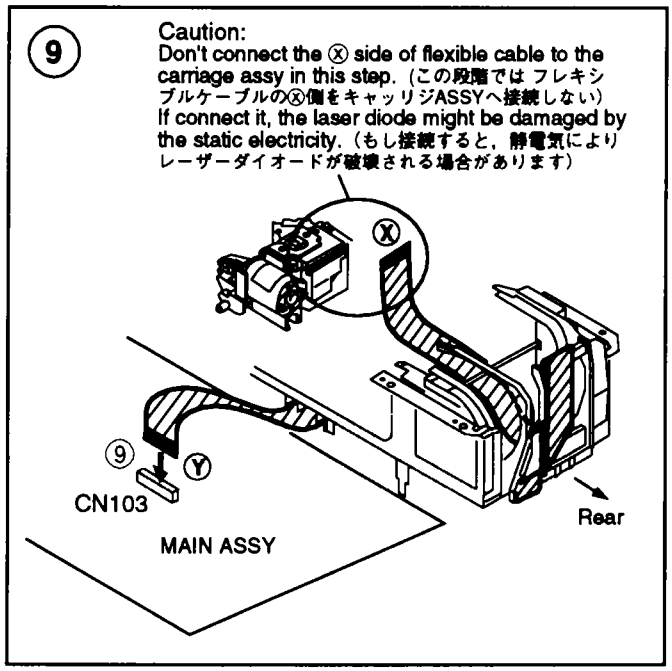


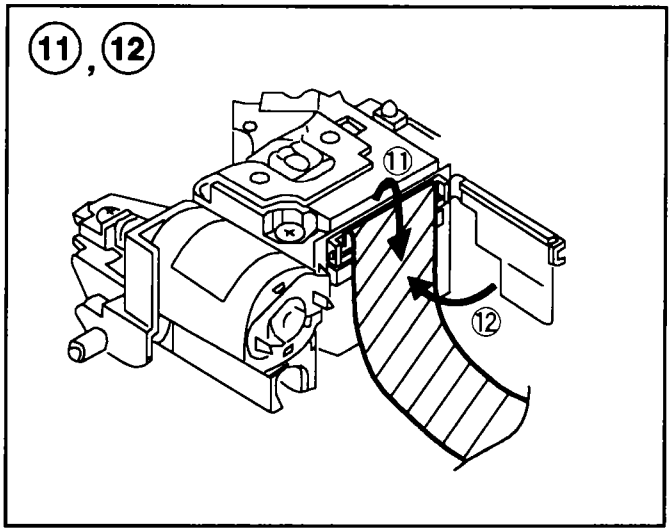
⑥, ⑦

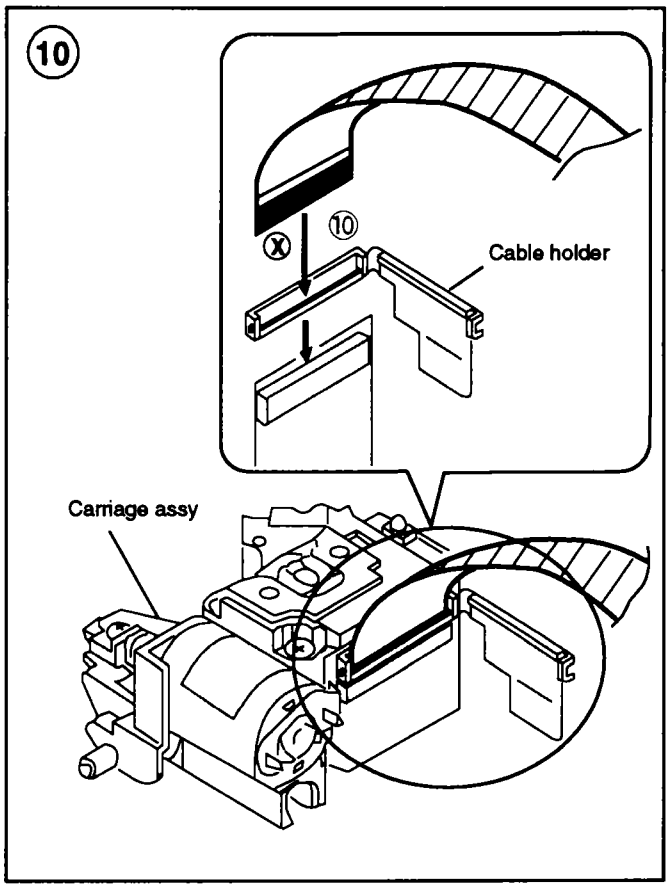


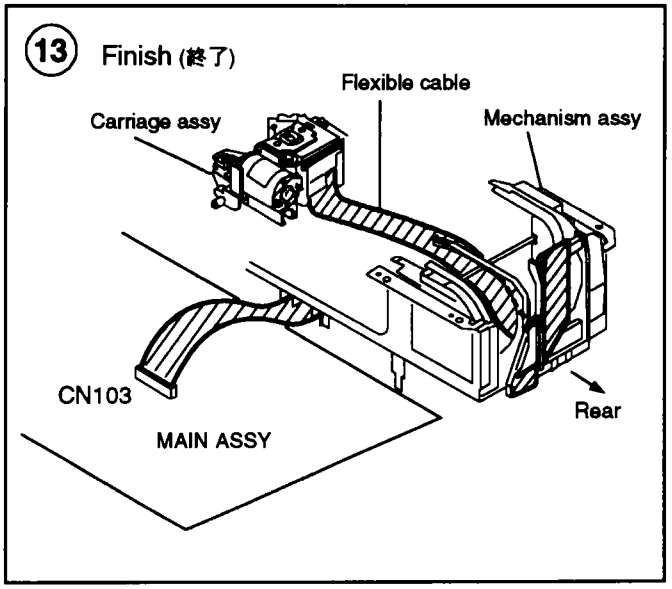
⑧ Turn the mechanism assy upside down
(メカASSYを裏返す)




9
Caution:
Don't connect the ⓧ side of flexible cable to the carriage assy in this step. (この段階では フレキシブルケーブルのⓧ側をキャッリジASSYへ接続しない)
If connect it, the laser diode might be damaged by the static electricity. (もし接続すると，静電気により レーザーダイオードが破壊される場合があります)
ⓧ
⑨
Ⓨ
CN103
MAIN ASSY
Rear


11, 12
⑪
⑫


10
ⓧ
⑩
Cable holder
Carriage assy


13 Finish (終了)
Flexible cable
Carriage assy
Mechanism assy
CN103
MAIN ASSY
Rear

9. IC INFORMATION

•The information in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

■PD3337A (FLKY ASSY : IC101)

• MODE CONTROL IC

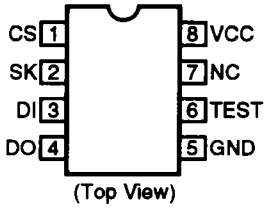
• Pin Function

No.	Mark	I/O	Pin Name	Function	No.	Mark	I/O	Pin Name	Function
1	VCC	I	VCC	+5V	33	P46/FS22	O	LED B	Side B LED output
2	P90/PWM	O	XRESET	Mother board reset output	34	P45/FS21	O	LED LD	LD tray OPEN/CLOSE LED output
3	P91/$\overline{SCK1}$	I/O	XSCK	Serial communication clock (Mech. controller, OSD IC, EEPROM)	35	P44/FS20	O	LED CD	LD tray OPEN/CLOSE LED output
4	P92/SI1	I	S M to F	Serial communication data input (Mech. controller, EEPROM)	36	P43/FS19	O	LED A	Side A LED output
5	P93/SO1	O	S F to M	Serial communication data output (Mech. controller, OSD IC, EEPROM)	37	P42/FS18	O	k	Display segment output
6	P94/$\overline{SCK2}$	O	XSCK	OSD IC chip select output (L : enable)	38	P41/FS17		j	
7	P95/SI2/$\overline{CS}$	O	–	Not used	39	P40/FS16		i	
8	P96/SO2				40	P50/FS15		h	
9	P97/UD	O	POWER ON	Mother board power supply switching output	41	P51/FS14		g	
10	AVCC	I	AVCC	+5V	42	P52/FS13		f	
11	P00/AN0	I	KEY3	Key data input	43	P53/FS12		e	
12	P01/AN1		KEY2		44	P54/FS11		d	
13	P02/AN2		KEY1		45	P55/FS10		c	
14	P03/AN3	I	–	Not used	46	P56/FS9		b	
15	P04/AN4				47	P57/FS8		a	
16	P05/AN5	I	SW1		48	P17/Vdisp	I	Vdisp	-29V power supply for VFD
17	P06/AN6		SW2		49	P60/FD0/FS7	O	G10	Display grid output
18	P07/AN7		SW3		50	P61/FD1/FS6		G9	
19	AVSS	I	AVSS	GND	51	P62/FD2/FS5		G8	
20	TEST	I	TEST	Connect to GND (Not used)	52	P63/FD3/FS4		G7	
21	X1	I	X1	NC (Not used)	53	P64/FD4/FS3		G6	
22	X2	I	X2	Connect to +5V (Not used)	54	P65/FD5/FS2		G5	
23	VSS	I	VSS	GND	55	P66/FD6/FS1		G4	
24	OSC1	I	OSC1	Connect a system clock oscillator	56	P67/FD7/FS0		G3	
25	OSC2	O	OSC2		57	P70/FD8		G2	
26	$\overline{RES}$	I	XRESET	CPU reset (L : Reset)	58	P71/FD9		G1	
27	P10/$\overline{IRQ0}$	I/O	SHAKE	Mechanism control serial communication request	59	P72/FD10	O	LED DOF	DISPLAY OFF LED output
28	P11/$\overline{IRQ1}$	I	SEL IR	Remote control input	60	P73/FD11	O	LED QTN	QUICK TURN LED output
29	P14/$\overline{IRQ4}$	I	FSX	EFM decoder 7.35MHz frame sync signal	61	P74/FD12	O	LED HQ	HQ CIRCUIT LED output
30	P15/$\overline{IRQ5}$/ TMOE	I	EFLG	EFM decoder error correction state signal	62	P75/FD13	O	–	Not used
31	P16/$\overline{EVENT}$	I	GND	GND	63	P76/FD14	O	ROMCS	EEPROM chip select output (H : Enable)
32	P47/FS23	O	WDF	For WATCHDOG pulse output	64	P77/FD15	O	–	Not used

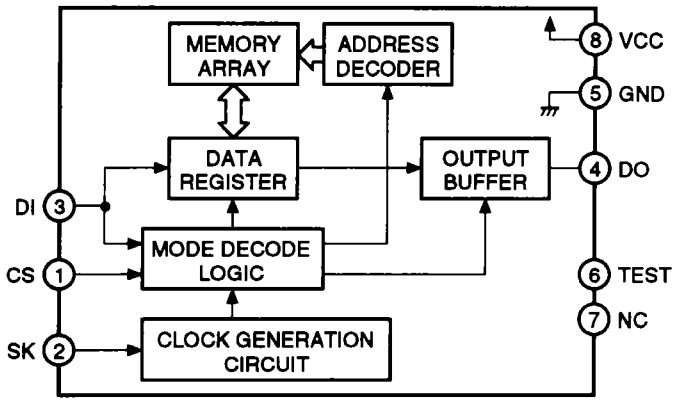
■AT93C46-10PC (FLKY ASSY : IC102)

- CMOS 1kbit EEPROM

• Pin Assignment



• Block Diagram



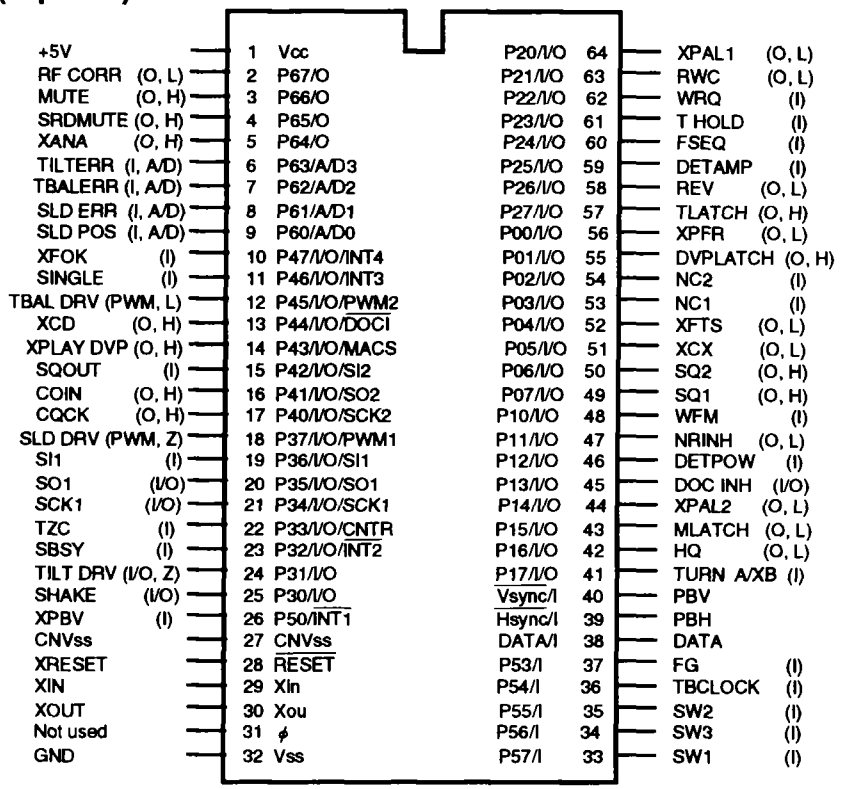
•Pin Function

No.	Pin Name	Function
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	GND
6	TEST	Test :Use by open (Connect to VCC or GND may do)
7	NC	No connect
8	VCC	Power supply

■PD0237A2 (MAIN ASSY : IC101)

• MECHANISM CONTROL IC

•Pin Assignment (Top View)


+5V 1 Vcc
RF CORR (O, L) 2 P67/O
MUTE (O, H) 3 P66/O
SRDMUTE (O, H) 4 P65/O
XANA (O, H) 5 P64/O
TILTERR (I, A/D) 6 P63/A/D3
TBALERR (I, A/D) 7 P62/A/D2
SLD ERR (I, A/D) 8 P61/A/D1
SLD POS (I, A/D) 9 P60/A/D0
XFOK (I) 10 P47/I/O/INT4
SINGLE (I) 11 P46/I/O/INT3
TBAL DRV (PWM, L) 12 P45/I/O/PWM2
XCD (O, H) 13 P44/I/O/DOCI
XPLAY DVP (O, H) 14 P43/I/O/MACS
SQOUT (I) 15 P42/I/O/SI2
COIN (O, H) 16 P41/I/O/SO2
CQCK (O, H) 17 P40/I/O/SCK2
SLD DRV (PWM, Z) 18 P37/I/O/PWM1
SI1 (I) 19 P36/I/O/SI1
SO1 (I/O) 20 P35/I/O/SO1
SCK1 (I/O) 21 P34/I/O/SCK1
TZC (I) 22 P33/I/O/CNTR
SBSY (I) 23 P32/I/O/INT2
TILT DRV (I/O, Z) 24 P31/I/O
SHAKE (I/O) 25 P30/I/O
XPBV (I) 26 P50/INT1
CNVss 27 CNVss
XRESET 28 RESET
XIN 29 Xin
XOUT 30 Xou
Not used 31 φ
GND 32 Vss
P20/I/O 64 XPAL1 (O, L)
P21/I/O 63 RWC (O, L)
P22/I/O 62 WRQ (I)
P23/I/O 61 T HOLD (I)
P24/I/O 60 FSEQ (I)
P25/I/O 59 DETAMP (I)
P26/I/O 58 REV (O, L)
P27/I/O 57 TLATCH (O, H)
P00/I/O 56 XPFR (O, L)
P01/I/O 55 DVPLATCH (O, H)
P02/I/O 54 NC2 (I)
P03/I/O 53 NC1 (I)
P04/I/O 52 XFTS (O, L)
P05/I/O 51 XCX (O, L)
P06/I/O 50 SQ2 (O, H)
P07/I/O 49 SQ1 (O, H)
P10/I/O 48 WFM (I)
P11/I/O 47 NRINH (O, L)
P12/I/O 46 DETPOW (I)
P13/I/O 45 DOC INH (I/O)
P14/I/O 44 XPAL2 (O, L)
P15/I/O 43 MLATCH (O, L)
P16/I/O 42 HQ (O, L)
P17/I/O 41 TURN A/XB (I)
Vsync/I 40 PBV
Hsync/I 39 PBH
DATA/I 38 DATA
P53/I 37 FG (I)
P54/I 36 TBCLOCK (I)
P55/I 35 SW2 (I)
P56/I 34 SW3 (I)
P57/I 33 SW1 (I)

•Pin Function

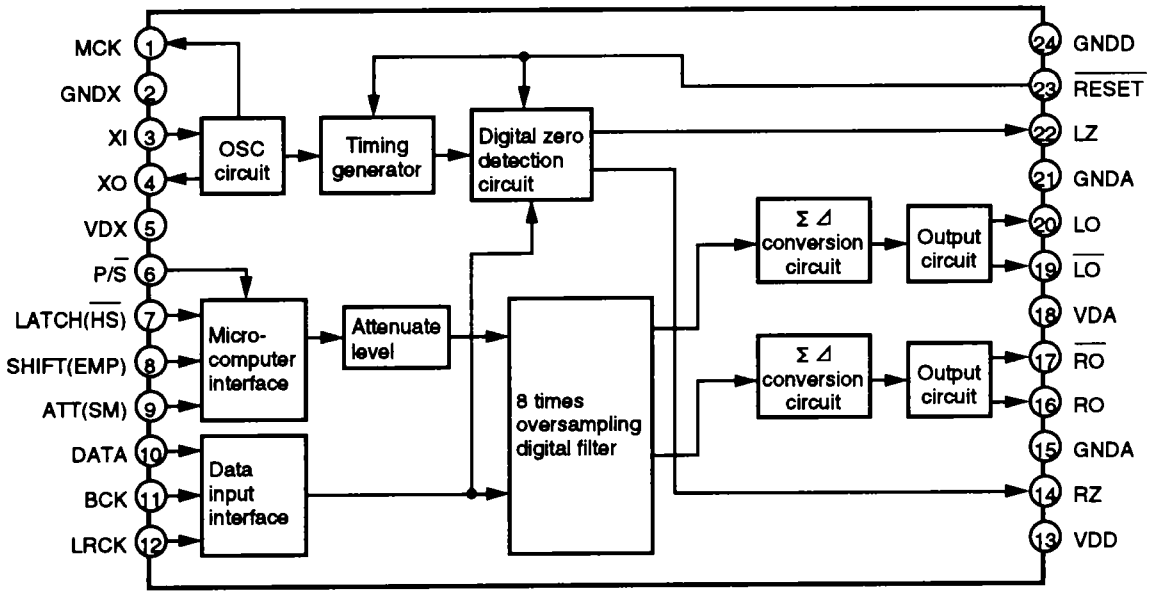
No.	Pin name	I/O	Function
1	Vcc	I	Power supply connection pin. 5V±10% applied.
2	RF CORR	O	RF correction switch signal output pin. H = Gain up H = Rise up CAV, within #8000 at TOC reading. L = Others (#8000 - #8100 : hold the previous state)
3	MUTE	O	Audio system audio mute control signal output pin. H = Mute ON, L = Mute OFF
4	SRDMUTE	O	AC3 mute control signal output pin. Release mute only during play. L = Mute, H = Release mute
5	XANA	O	Digital/Analog audio switching signal output pin. H = Digital, L = Analog
6	TILT ERR	I A/D	Tilt sensor output signal input pin. The tilt motor is controlled to make this signal 2.5V.
7	TBAL ERR	I A/D	Tracking balance error signal input pin. (A/D input port) This signal is converted from analog to digital and used for tracking offset control input.
8	SLD ERR	I A/D	Slider error signal input pin. (A/D input port) This signal is converted from analog to digital and used for slider servo control input.
9	SLD POS	I A/D	Pickup position detection switch input pin. (A/D input port) The switches are resistance divided, the A/D input value read in, and the position detected.
10	XFOK	I	Focus servo lock signal input pin. L = Lock, H = Unlock Used for focus servo lock detection.
11	SINGLE	I	ATT switch in single mode and communicates this data to the mode controller. L = Normal, H = Single
12	TBAL DRV	O PWM	Tracking offset control signal output pin. PWM outputs the tracking offset for use as the auto tracking offset. Period 910 μsec, tri-state control : H, L, Z
13	XCD	O	LD/CD switching signal output pin.
14	XPLAY DVP	O	Spindle servo signal output pin. L = During servo, H = Acceleration, brake, during servo
15	SQOUT	I	DSP reading command data input pin. SUBQ is read out.
16	COIN	O	DSP writing command data output pin.
17	CQCK	O	DSP read/write command clock output pin. Read in at rising edge.
18	SLD DRV	O PWM	Slider control signal output pin. Side A : 5V = FWD, 0V = REV, Side B : 0V = FWD, 5V = REV, 2.5V = STOP, Period 910 μsec, tri-state control : H, L, Z

No.	Pin Name	I/O	Function
19	SI1	I	Data input pin from mode controller IC.
20	SO1	O	Serial data output pin to mode controller IC.
21	SCK1	I/O	Clock for serial communication with mode controller IC. Other than when communicating with mode controller IC, input mode.
22	TZC	I	Tracking error zero cross signal pin. Control the slider motor which is counted this signal in the track count search.
23	SBSY	I	Subcode block sync. signal input pin. H = S0, S1, L = Others
24	TILT DRV	I/O	Load/tilt control output pin. 0.5V - tray in, out/tilt down, up 2.5V - stop Use for tilt servo by PWM output the tilt drive.
25	SHAKE	I/O	Handshake signal pin for data communications with mode controller IC. This pin is a bidirectional data line and control the input/output by the respective microcomputers.
26	XPBV	I	LD/CDV playback vertical sync signal input pin. L = During vertical sync
27	CN Vss	I	Ground for A/D conversion.
28	XRESET	I	Reset signal input pin. L = Reset, H = Release reset Controlled by mode controller.
29	XIN	I	9MHz clock oscillation input pin.
30	XOUT	O	9MHz clock oscillation output pin.
31	N.C.	O	Dedicated output pin, so other uses prohibited.
32	Vss	I	Ground.
33	SW1	I	Switch input pin for loading/tilt position detection.
34	SW3	I	Switch input pin for loading/tilt position detection.
35	SW2	I	Switch input pin for loading/tilt position detection.
36	TBCLOCK	I	Spindle lock signal input pin. H = Lock, L = Unlock
37	FG	I	Spindle motor FG signal input pin . 16 pulses per rotation, used within microcomputer frequency divided by 2.
38	DATA	I	Mechanism controller built-in Phillips code/decode input pin.
39	XPBH	I	Playback HSYNC input for Phillips coding/decoding.
40	XPBV	I	Playback VSYNC input for Phillips coding/decoding.
41	TURN A/XB	I	Double sided mech. turn switch. H = Side A , L = Side B
42	HQON	O	High quality circuit (analog NR) control signal output pin. H = Through the HQ circuit, L = Not through
43	MLATCH	O	PD4596 serial latch signal output pin. Latches at rising edge.
44	XPAL2	O	NTSC/PAL circuit switching signal output excepting VDEM . H = NTSC, L = PAL
45	DOC INH	I/O	Control the clamp pulse and clamp killer circuits by tri-state.
46	DETPOW	I	Used as power supply abnormality signal input port. L = Normal, H = Abnormal
47	NRINH	O	VDEM noise reduction control output pin. L = Normal, H = No NR
48	WFM	I	Field discrimination signal from DVP. H = ODD
49	SQ1	O	Analog audio switching signal output pin. 1/L Squelch : H
50	SQ2	O	Analog audio switching signal output pin. 2/R Squelch : H
51	XCX	O	Analog audio CX noise reduction switching signal output pin. L= ON, H = OFF
52	XFTS	O	Serial communication switching signal output to the DSP/other IC. L = DSP, H = Excepting DSP
53	N.C.1	O	Uses prohibition at high speed communication.
54	N.C.2		
55	DVPLATCH	O	PD6159 serial latch signal output pin. Latches at falling edge.
56	XPFR	O	17MHz PLL control signal output pin. H = Compare the phase L = Free running
57	TLATCH	O	Latch output of serial control for DAC & digital filter IC PD2026A . Latches at falling edge.
58	REV	O	Pickup tension signal output pin at reverse. H = Side B , L = Side A
59	DETAMP	I	Spindle overcurrent detection signal input pin. L = Overcurrent, H = Normal
60	FSEQ	I	Subcode sync match detection signal input pin. H = Matches, L = Does not match
61	THOLD	I	Track jump accelerating/decelerating signal input pin. H = Accelerating/decelerating , L = Neither
62	WRQ	I	Subcode Q read OK signal input pin. L = NG , H = OK This pin goes high when the subcode Q data passes the CR check.
63	RWC	O	DSP read/write command signal output pin. L = Read, H = Write
64	XPAL	O	PAL/NTSC switching signal output pin for VDEM. H = NTSC, L = PAL

■TC9004F (MAIN ASSY : IC201)

• D/A CONVERTER

•Block Diagram



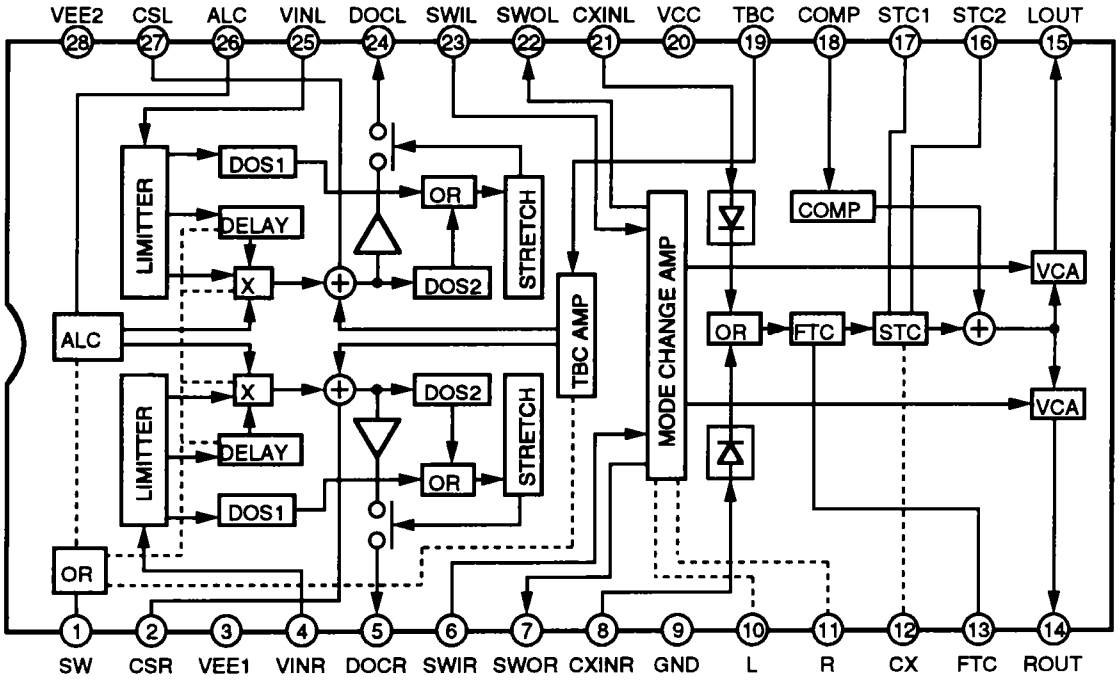
•Pin Function

No.	Pin name	I/O	Function
1	MCK	O	System clock supply pin
2	GNDX	—	Ground pin of oscillation section
3	XI	I	Crystal oscillator connection pin. Generates a clock for system.
4	XO	O	
5	VDX	—	Power supply pin for oscillation section
6	P/$\overline{S}$	I	Parallel/serial control switching pin (Schmitt input and pull-up resistor)
7	LATCH ($\overline{HS}$)	I	In the serial control, data latch signal input pin for attenuator. In the parallel control, normal/double speed mode selection pin. (Schmitt input and pull-up resistor)
8	SHIFT (EMP)	I	In the serial control, shift clock input pin for attenuator. In the parallel control, deemphasis filter ON/OFF control pin. (Schmitt input and pull-up resistor)
9	ATT (SM)	I	In the serial control, data I input pin for attenuator. In the parallel control, soft mute control pin. (Schmitt input and pull-up resistor)
10	DATA	I	Data input pin (Schmitt input)
11	BCK	I	Bit clock input pin (Schmitt input)
12	LRCK	I	LR clock input pin (Schmitt input)
13	VDD	—	Power supply pin for digital section
14	RZ	O	R-ch digital zero detection output pin
15	GNDA	—	Ground pin for R-ch analog section
16	RO	O	R-ch data positive-phase output pin
17	$\overline{RO}$	O	R-ch data negative-phase output pin
18	VDA	—	Power supply pin for analog section
19	$\overline{LO}$	O	L-ch data negative-phase output pin
20	LO	O	L-ch data positive-phase output pin
21	GNDA	—	Ground pin for L-ch analog section
22	LZ	O	L-ch digital zero detection output pin
23	$\overline{RESET}$	I	Reset signal input pin
24	GND	—	Ground pin

■PA0061AM (MAIN ASSY : IC351)

• A. AUDIO DEMODULATION

• Block Diagram



•Pin Function

No.	Pin name	Function
1	SW	PAL/NTSC switch pin
2	CSR	Capacitor connection pin for eliminating carrier
3	VEE1	Power supply pin
4	VINR	FM signal input pin
5	DOCR	Drop out correction switch output pin
6	SWIR	Mode switch amp input pin
7	SWOR	Mode switch amp output pin
8	CXINR	CX control signal input pin
9	GND	Ground
10	L	Mode switch pin L
11	R	Mode switch pin R
12	CX	CX ON-OFF switch pin
13	FTC	Capacitor connection pin for FTC
14	ROUT	R ch output pin
15	LOUT	L ch output pin
16	STC2	STC pih 2
17	STC1	STC pin 1
18	COMP	Compensator pin
19	TBC	TBC error signal input pin
20	VCC	Power supply pin
21	CXINL	CX control signal input pin
22	SWOL	Mode switch amp output pin
23	SWIL	Mode switch amp input pin
24	DOCL	Drop out correction switch output pin
25	VINL	FM signal input pin
26	ALC	Capacitor connection pin for ALC
27	CSL	Capacitor connection pin for eliminating carrier
28	VEE2	Power supply pin

• Truth Table of Mode Switch

MODE	SW (pin1)
PAL	Low (0V)
NTSC	High (5V)

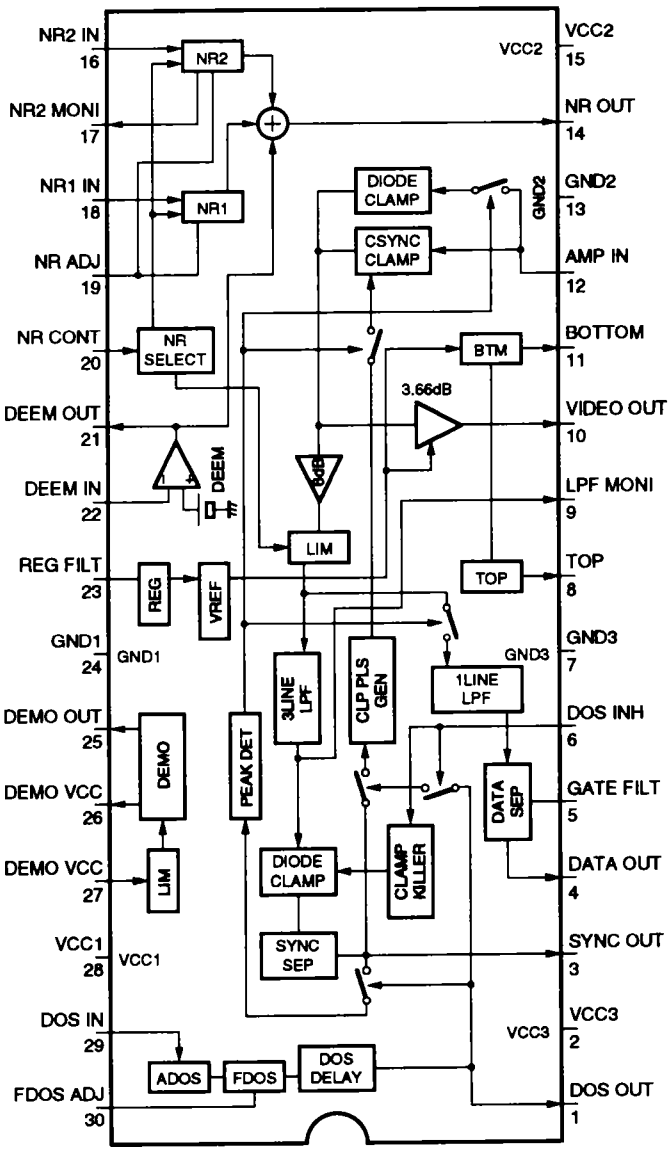
MODE	L (pin 10)	R (pin 11)
STEREO	Low (0V)	Low (0V)
MONO (L)	Low (0V)	High (5V)
MONO (R)	High (5V)	Low (0V)
SQUELCH	High (5V)	High (5V)

MODE	CX (pin 12)
CX ON	Low (0V)
CX OFF	High (5V)

■LA7133 (MAIN ASSY : IC400)

• VIDEO IC

•Block Diagram



•Pin Function

No.	Pin Name	Function
1	DOS OUT	Drop out pulse output
2	VCC3	VCC for SYNC SEP section
3	SYNC OUT	Composite sync output
4	DATA OUT	Data pulse output
5	GATE FILT	Connect a capacitor for Date-Gate
6	DOS INH	Clamp pulse and clamp killer control
7	GND3	GND for SYNC SEP section
8	TOP	Reference DC (TOP) for A/D
9	LPF MONI	Monitor the LPF for SYNC SEP
10	VIDEO OUT	Signal output for A/D
11	BOTTOM	Reference DC (BOTTOM) for A/D
12	AMP IN	Sync chip clamp input
13	GND2	GND for VIDEO
14	NR OUT	Noise reduction output
15	VCC2	VCC for VIDEO section
16	NR2 IN	Signal input (2) for noise reduction
17	NR2 MONI	Limitter output for noise reduction
18	NR1 IN	Signal input (1) for noise reduction
19	NR ADJ	Limitter level adjusting pin for noise reduction
20	NR CONT	Noise reduction (1, 2) select and limitter control
21	DEEM OUT	De emphasis output
22	DEEM IN	De emphasis input
23	REG FILT	Connect a capacitor for regulator
24	GND1	GND for RF section
25	DEMO OUT	Demodulation output of RF signal
26	DEMO VCC	VCC for FM demodulation output
27	DEMO IN	RF input for FM demodulation
28	VCC1	VCC for RF section
29	DOS IN	RF input for DOS
30	FDOS ADJ	FDOS sensitivity adjustment

■ PD6159A (MAIN ASSY : IC500)

• DUAL DIGITAL VIDEO PROCESSOR IC

• Descriptions

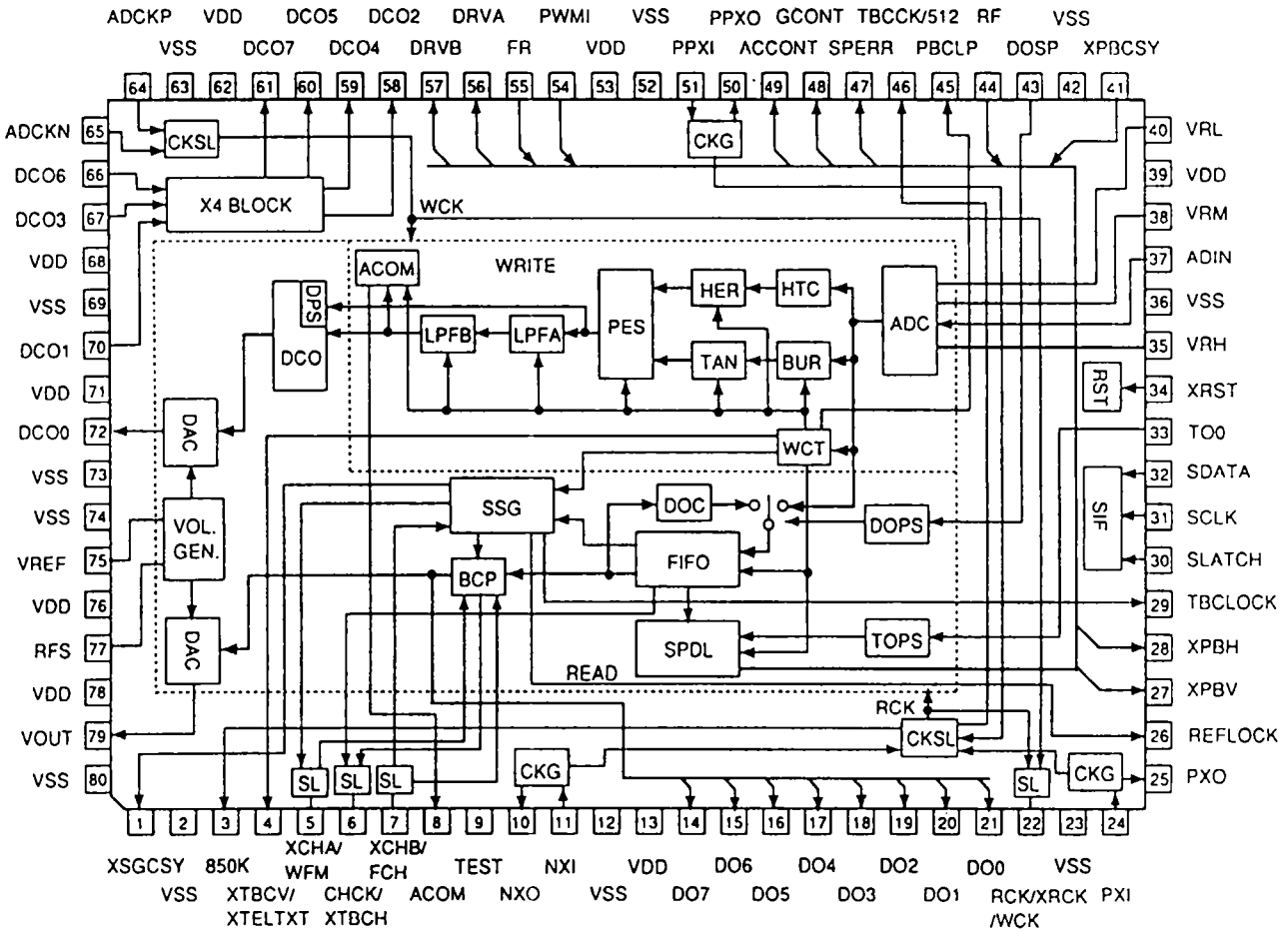
The PD6159A is a digital video signal processor (DVP) IC designed for dual-CLD players. It supplies time-base-corrected (TBC) video signals (conforming to both PAL and NTSC formats), which have a jitter right after the RF demodulation. It also generates sync signals which synchronize with these output video signals. In addition, various signals required for spindle control are generated by the IC. The PD6159A features the following.

The main functions are compatible with those of the PD0146A (NTSC-exclusive DVP).

Clocks NTSC : 4 fsc
PAL : 4 fp (4x pilot burst for disc video)
4 fsc (for squelch)

Digital TBC
Sync signal generation and synchronization
Generation of a signal for spindle control
Dropout compensation NTSC : Color
PAL : Monochrome
Character-superimpose function
Blue-background generation

• Block Diagram



• Pin Function

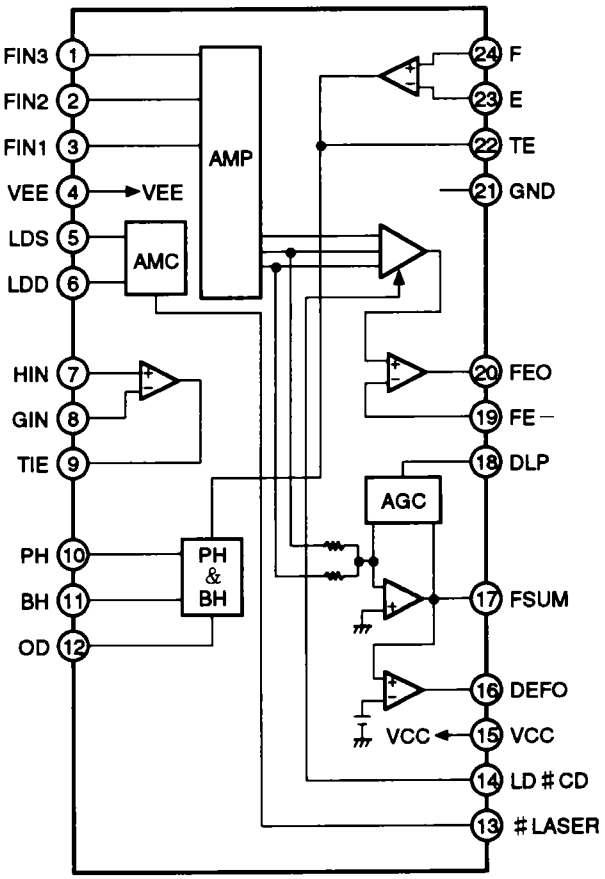
No.	Pin Name	I/O	Function	
1	XSGCSY	O	Outputs the reference composite sync from SG with negative logic. While normally in synchronization with the output video signal, it can be specified for free run in memory system mode. (Always synchronized in squelch mode) It can also be delayed by a command with a specified delay duration (SYD0-5).	
2	VSS	–	To be connected to GND (VSS associated with the logic)	
3	850K	O	Output obtained by exclusive-ORing the NTSC fsc wave with the PAL fsc wave. After passing through an external filter, it can be used as an 850-kHz wave required for NTSC-to-PAL conversion.	
4	XTBCV	O	TELSEL=0	Outputs time-base-corrected V sync with negative logic. In PAL, the timing of the rising can be set to the ends of 23H and 336H by a command (XTBCVSEL).
	XTELTXT	O	TELSEL=1 & NTSC/XPAL=0	Outputs "L" to indicate the teletext data positions (video portion at 20H, 21H, 333H, 334H) in PAL. Fixed to "H" in NTSC.
5	XCHA	I	XCGEN=0	To be connected to the character output of the OSD IC when using the character-superimpose function. When "L" the white level is imposed to the video output.
	WFM	O	XCGEN=1	Outputs "H" for the first field and "L" for the second field
6	CHCK	O	XCGEN=0	Outputs 2-fsc (2-fp) waves for the OSD IC when using the character-superimpose function. It is synchronized with the RCK/XRCK output.
	XTBCH	O	XCGEN=1	Outputs the time-base-corrected H sync with negative logic
7	XCHB	I	XCGEN=0	Accepts the character-frame output of the OSD IC when using the character(-frame)-superimpose function. When the input to this pin is "L" and to XCHA is "H" the gray level is imposed on the video output.
	FCH	I	XCGEN=1 & MEMSYS=1	Accepts the field-change signal from the memory controller in memory system mode "H" at 268H in NTSC or "H" at 315H in PAL during the second field switches the second field to the first field. To be fixed to "L" when not used.
8	ACOM	O	Outputs a signal representing the duty, which depends on the error level obtained at the internal phase comparator. To be used for audio jitter compensation.	
9	TEST	I	To be used when testing the IC Fix it to "L"	
10	NXO	O	To be connected to the NTSC 4-fsc crystal oscillator	
11	NXI	I	To be connected to the NTSC 4-fsc crystal oscillator	
12	VSS	–	To be connected to GND (VSS associated with the logic)	
13	VDD	–	To be connected to +5 V (VDD associated with the logic)	
14	DO7	O	To be used normally when OE=1 and OSD0/OSD01=0 A time-base-corrected digital video signal is obtained here in memory mode. DO0 yields the LSB and DO7 the MSB. The signal is in synchronization with the RCK/XRCK output. The squelch data will be output in squelch mode. The data to be output can be selected by commands OSD0/OSD1. When OE=0, these pins are fixed to "L".	
15	DO6			
16	DO5			
17	DO4			
18	DO3			
19	DO2			
20	DO1			
21	DO0			
22	RCK/XRCK	O	OTHERS	Outputs the reference clock (4 fsc for NTSC, 4 fp for PAL video, or 4 fsc for PAL squelch) Positive or negative phase can be selected by a command (RCKSEL).
	WCK	O	OE=1 & OSD=1	Outputs the write clock (4 fsc for NTSC or 4fp for PAL)
23	VSS	–	To be connected to GND (VSS associated with the logic)	
24	PXI	I	To be connected to the PAL 4-fsc crystal oscillator	
25	PXO	O	To be connected to the PAL 4-fsc crystal oscillator	
26	REFLOCK	O	Outputs "H" when the phase difference of H/V sync associated with PB (after TBC) and those associated with SSG is small enough.	
27	XPBV	O	Outputs the signal obtained by separating V sync from the signal at XPBCSY (pin 41) with negative logic.	
28	XPBH	O	Outputs the signal obtained by separating H sync from the signal at XPBCSY (pin 41) with negative logic.	
29	TBCLOCK	O	Outputs "H" when the spindle loop and the TBS loop are locked	
30	SLATCH	I	Gives the latch timing for data applied to the serial interface (Through at the rising and no change in register contents during L/H periods and at the falling.)	
31	SCLK	I	Clock inputs for the serial interface. The SDATA value will be read at the rising edge.	
32	SDATA	I	Provides the serial interface with data	
33	TO0	I	Accepts a tracking-open pulse. The pulse will be internally stretched. The stretch volume is set by a command (STD0 to STD3).	
34	XRST	I	Input for initializing the IC. When "L" all the registers and counters of the IC are set to their initial values.	
35	VRH	I	Provides the AC converter with the reference voltage of the H side	
36	VSS	–	To be connected to GND (VSS for the AD converter)	
37	ADIN	I	Input for the AD converter. Accepts a composite video signal having a jitter. In PAL, the pilot burst wave must be in a range of the half the difference between the H reference voltage and the L reference voltage. (See the example of input specifications.)	
38	VRM	I	Intertap pin between the reference resistors. A bypass capacitor can be connected for stabilization.	

No.	Pin Name	I/O	Function
39	VDD	–	To be connected to +5 V (VDD for the AD converter)
40	VRL	I	Provides the AD converter with the reference voltage for the L side
41	XPBCSY	I	The PB composite sync is to be supplied here with negative logic
42	VSS	–	To be connected to GND (VSS associated with the logic)
43	DOSP	I	Accepts the dropout detection pulse. The pulse will be internally stretched. The stretch volume is set by a command (STD0-3).
44	RF	I	Accepts an RF signal for the spindle servo
45	PBCLP	O	Flag output to indicate the positions for level clamp of the pilot-burst signal in PAL. (See the example of input specifications.)
46	TBCCK/512	O	Outputs a 1/512th division (approx. 28 kHz) of the clock (NTSC: 4 fsc, PAL: 4 fp) used for TBC It is used to generate a chopping wave for spindle control.
47	SPERR	O	Output pin for a phase-frequency error of the spindle errors. It outputs the result of comparison between PBH and reference H in tristate. The polarity can be set by a command (PERPOL).
48	GCONT	O	Outputs a PWM signal according to the command-specified value (CD0-3)
49	ACCONT	O	Tristate output of the acceleration/deceleration signal, which depends either on the forced acceleration/deceleration signal, the error detection by RF or error detection by H sync. The acceleration/deceleration volume is determined by setting the duty of the PWM output by commands (RFGD0-3, HFGD0-3). The polarity can be set by a command (ACCPOL).
50	PPXO	O	To be connected to the PAL 4-fp crystal oscillator
51	PPXI	I	To be connected to the PAL 4-fp crystal oscillator
52	VSS	–	To be connected to GND (VSS associated with the logic)
53	VDD	–	To be connected to +5 V (VDD associated with the logic)
54	PWMI	I	Accepts a signal obtained through the voltage comparison between the spindle error which has passed through a loop filter and the chopping wave externally generated from TBCCK/512.
55	FR	I	Accepts a signal obtained through the voltage comparison between the spindle error which has passed through a loop filter and the destination voltage.
56	DRVA	O	Control signal output for Tr which drives the spindle motor. It is applicable to either a brush motor or brushless motor, selection of which is by a command (BLM). (See the functional block diagram for the logic.)
57	DRVB	O	
58	DCO2	O	Outputs a signal obtained through waveformshaping of the DCO1 signal
59	DCO4	O	Outputs a signal obtained through waveformshaping of the DCO3 signal
60	DCO5	O	Outputs a signal multiplied by 2
61	DCO7	O	Outputs a signal multiplied by 4, which is used as the write clock after passing through a 4-fp or 4-fsc filter.
62	VDD	–	To be connected to +5 V (VDD for output multiplied by 4)
63	VSS	–	To be connected to GND (VSS for output multiplied by 4)
64	ADCKP	I	Write clock input for PAL. Accepts the DCO7 output via a 4-fp filter.
65	ADCKN	I	Write clock input for NTSC. Accepts the DCO7 output via a 4-fsc filter.
66	DCO6	I	Accepts a signal obtained by delaying the DCO5 signal by approx. 35 ns
67	DCO3	I	Accepts a signal obtained by delaying the DCO2 signal by approx. 70 ns
68	VDD	–	To be connected to +5 V (VDD for input multiplied by 4)
69	VSS	–	To be connected to GND (VSS for input multiplied by 4)
70	DCO1	I	Accepts the DCO0 signal via a low-pass filter
71	VDD	–	To be connected to +5 V (VDD for the DA converter for DCO0 output)
72	DCO0	O	DC0 output . The signal here is multiplied by 4 to produce ADCK It can be fixed to the minimum potential by a command (DCOINH).
73	VSS	–	To be connected to GND (VSS for the DA converter for DCO0 output)
74	VSS	–	To be connected to GND (VSS for the internal power source for the DA converter)
75	VREF	I	Input to show the reference voltage to the internal power source for the DA converter
76	VDD	–	To be connected to +5 V (VDD for the internal power source for the DA converter)
77	RFS	IO	Pin to specify the internal current of the internal power source for the DA converter Connect 5.1 kohms as standard between this pin and GND.
78	VDD	–	To be connected to +5 V (VDD for the DA converter for VOUT output)
79	VOUT	O	Time-base-corrected video output. While a composite sync is normally inserted, the sync position will be found at the pedestal level in memory system mode. (However, some half-H pulses etc. may partly remain near V sync.)
80	VSS	–	To be connected to GND (VSS for the DA converter for VOUT output)

■LA9425 (MAIN ASSY : IC801)

- TRKG, FOCUS AND TILT ERROR AMP.

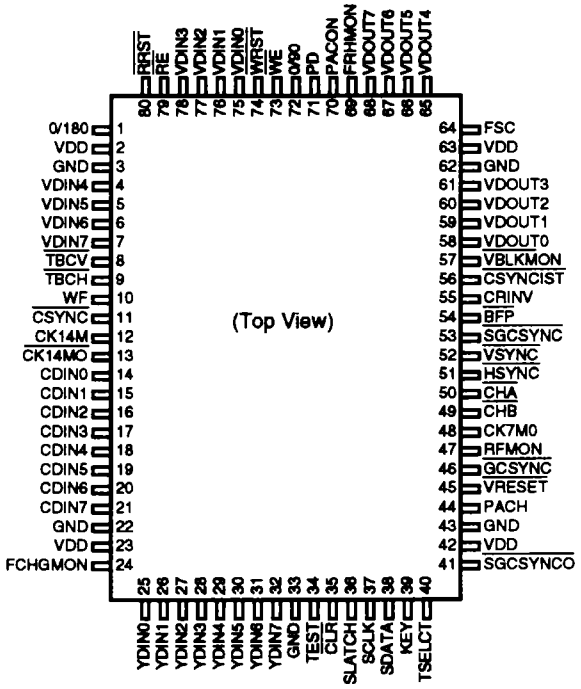
• **Block Diagram**



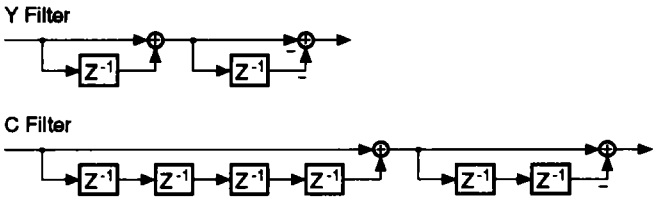
■PD4596A (DMYC ASSY : IC101)

• MEMORY CONTROLLER IC

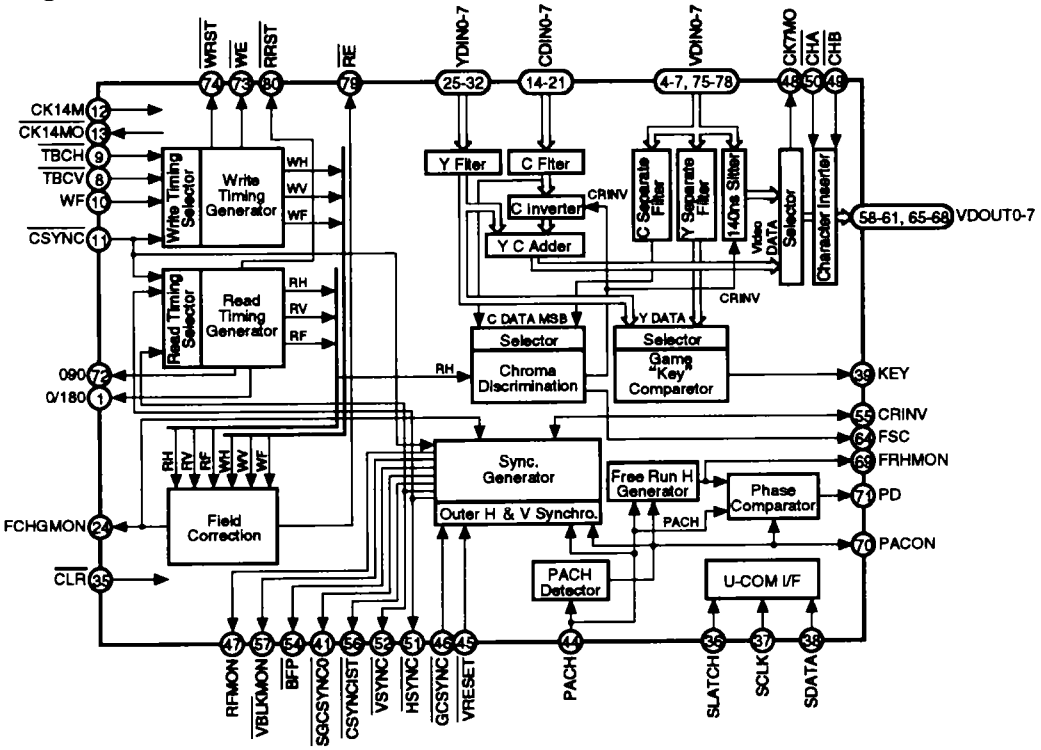
•Pin Assignment (Top View)



•Filter Specification



•Block Diagram



•Pin Function

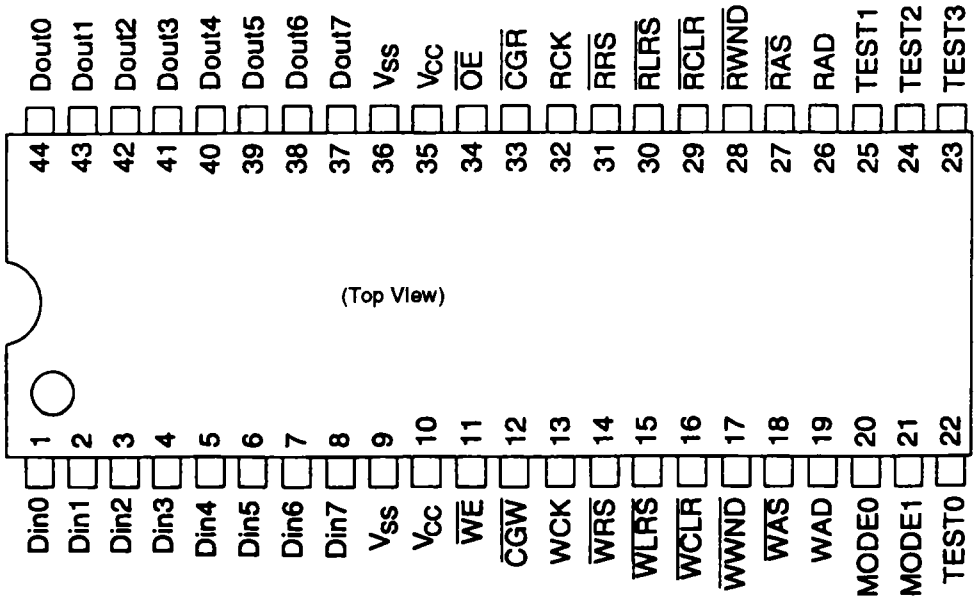
No.	Mark	I/O	Pin Name	Function
1	0/180	O	0/180 signal output (P/N=0)	Outputs 0/180 signal at PAL trick play
		I	Sync insertion (P/N=1)	Set to "H" when sync inserting into the IC. Switchable the sync insertion ON/OFF with the microcomputer command at "L".
2	VDD	—	Power supply pin	Connect to +5V
3	GND	—	Ground pin	Connect to GND
4	VDIN4	I	Video data input	Inputs upper 4 bit data output of the field memory. VDIN0 (pin 75) : LSB, VDIN7 (pin 7) : MSB
5	VDIN5			
6	VDIN6			
7	VDIN7			
8	$\overline{TBCV}$	I	TBC V sync input	Inputs time-base-corrected V sync with negative logic from DVP. Use for write control of the field memory.
9	$\overline{TBCH}$	I	TBC H sync input	Inputs time-base-corrected H sync with negative logic from DVP. Use for write control of the field memory.
10	WF	I	Field input of write system	Inputs field monitor signal from DVP. H=1st field, L=2nd field Use for write control of the field memory.
11	$\overline{CSYNC}$	I	Composite sync input of reference system	Inputs composite sync of the reference system with negative logic from DVP. Use for write control at squelch, read control at PAL and read/write control at 3D.
12	CK14M	I	Clock input	Clock input
13	$\overline{CK14MO}$	O	14MHz inversion clock output	Clock output which is inverted the CK14M input
14	CDIN0	I	Chroma data input 0	Inputs chroma data output in the Y/C SEP IC is used CNIN0 (pin 14) : LSB, CDIN7 (pin 21) : MSB
15	CDIN1		Chroma data input 1	
16	CDIN2		Chroma data input 2	
17	CDIN3		Chroma data input 3	
18	CDIN4		Chroma data input 4	
19	CDIN5		Chroma data input 5	
20	CDIN6		Chroma data input 6	
21	CDIN7		Chroma data input 7	
22	GND	—	Ground pin	Connect to GND
23	VDD	—	Power supply pin	Connect to +5V
24	FCHGMON	O	Field change signal monitor output	Monitor output of the field change signal which switching the second field to first field in the internal sync generation section at NTSC. Use for the DVP field change signal at PAL.
25	YDIN0	I	Luminance data input 0	Inputs luminance data output in the Y/C SEP IC is used. YDIN0 (pin 25) : LSB, YDIN7 (pin 32) : MSB When output side is more than 9 bit, inputs the upper 8 bit. Fix to "L" when Y/C SEP IC is not used.
26	YDIN1		Luminance data input 1	
27	YDIN2		Luminance data input 2	
28	YDIN3		Luminance data input 3	
29	YDIN4		Luminance data input 4	
30	YDIN5		Luminance data input 5	
31	YDIN6		Luminance data input 6	
32	YDIN7		Luminance data input 7	
33	GND	—	Ground pin	Connect to GND
34	TEST	I	IC test input	Use for IC test. Set to open.
35	CLR	I	Clear input	IC initialize input . L = whole register and counter etc. become initial value.
36	SLATCH	I	Serial interface latch signal input	Apply a data latch timing which is input to serial interface.
37	SCLK	I	Serial interface clock input	Clock input for serial interface. Read in the SDATA value at the rising edge.
38	SDATA	I	Serial interface data input	Apply a data to serial interface.
39	KEY	O	Luminance key signal output	Compare the luminance level or luminance data input and register of the video data, then output the result L/H level. If input is larger than reference, output "L", and if input is smaller than reference, output "H".
40	TSELCT	I	Test mode selection input	Use for select the test mode in the IC TEST. Set to open.

No.	Mark	I/O	Pin Name	Function
41	$\overline{\text{SGCSYNC0}}$	O	Composite sync output of read system (No 140ns shift)	Outputs the composite sync from the internal sync generation section with negative logic at NTSC. Outputs CSYNC (pin 11) signal with delayed 4 clock at PAL and 2 clock at 3D.
42	VDD	–	Power supply pin	Connect to +5V
43	GND	–	Ground pin	Connect to GND
44	PACH	I	Game PACK H sync input	Inputs H sync from the game PACK with positive logic. Set to open when not synchronizing with game side.
45	$\overline{\text{VRESET}}$	I	Game PACK V reset input	Inputs V reset signal from the game PACK with negative logic. Set to open when not synchronizing with game side.
46	$\overline{\text{GCSYNC}}$	I	Game PACK composite sync input	Inputs composite sync from the game PACK with negative logic. Set to open when not synchronizing with game side.
47	RFMON	O	Read filter monitor output	Monitor output of field signal in the internal sync generation section. H : First field, L : Second field
48	CK7MO	O	7MHz clock output	Outputs a clock which is input clock divided by 2 from CK14M (pin 12). Ever time, reset by falling edge of H sync of the read system. (When H sync is falling edged, this clock is falling edge, too) Use for clock input of OSD IC.
49	$\overline{\text{CHB}}$	I	Character frame input	When using the character superimpose function, connect the character frame output of OSD IC. When this pin is "L" and CHA (pin 50) is "H", the gray level is imposed on the video data.
50	$\overline{\text{CHA}}$	I	Character input	When using the character superimpose function, connect the character output of OSD IC. When "L" the white level is imposed on the video data.
51	$\overline{\text{SGCSYNC}}$	O	H sync output of read system	Outputs H sync from the internal sync generation section with negative logic at NTSC.
52	$\overline{\text{VSYNC}}$	O	V sync output of read system	Outputs V sync from the internal sync generation section with negative logic.
53	$\overline{\text{SGCSYNC}}$	O	Composite sync output of read system	Outputs composite sync from the internal sync generation section with negative logic at NTSC. Perform the read control the field memory by this reference signal. Output this signal delayed by 1 clock with the video data output. HSYNC and VSYNC signals are synchronized.
54	$\overline{\text{BFP}}$	O	Burst flag pulse output	Outputs the pulse which is showed the color burst position on the video data output at NTSC. "L" period is the burst position.
55	CRINV	O	Chroma invert output (P/N=1)	It outputs the result of judgement of the chroma continuity from the video data input or the chroma data input.
		O	VSQ output (P/N=0)	Outputs "L" at microcomputer command XVSQ = 0 and "H" at XVSQ = 1, this signal output by latching with V of the read side.
56	$\overline{\text{CSYNCIST}}$	O	Sync output for insertion	Outputs for inserting the sync to the video signal after the D/A conversion.
57	$\overline{\text{VBLKMON}}$	O	V blanking period monitor output	Outputs V blanking period (half H period) from the internal sync generation section with negative logic at NTSC.
58	VDOUT0	O	Video data output 0	Outputs lower 4 bit of adding result between the video data input or luminance data and chroma data input, it output after 3 clocks as compared with the normal input.
59	VDOUT1		Video data output 1	
60	VDOUT2		Video data output 2	
61	VDOUT3		Video data output 3	
62	GND	–	Ground pin	Connect to GND
63	VDD	–	Power supply pin	Connect to +5V
64	FSC	O	FSC output	Outputs a clock which is input clock divided by 4 from CK14M (pin 12).
65	VDOUT4	O	Video data output 4	Outputs upper 4 bit of adding result between the video data input or luminance data and chroma data input.
66	VDOUT5		Video data output 5	
67	VDOUT6		Video data output 6	
68	VDOUT7		Video data output 7	
69	FRHMON	O	Free-run H sync monitor output	H sync monitor output of internal free-run H sync generation section
70	PACON	O	Game PACK H sync detection output	Outputs "H" by detecting the PACH signal input.
71	PD	O	Phase difference output between the PACH and free-run H	Outputs L/H pulse which is the phase difference between the PACH signal and H sync signal at rising edge of the internal free-run H sync generation section.
72	0/90	–	0/90 output pin	Outputs 0/90 signal at PAL trick play
73	$\overline{\text{WE}}$	O	Write enable output	Control the write operation of field memory
74	$\overline{\text{WRST}}$	O	Write reset output	Outputs signal for initializing the write address of field memory
75	VDIN0	I	Video data input 0	Inputs lower 4 bit data output of field memory
76	VDIN1	I	Video data input 1	
77	VDIN2	I	Video data input 2	
78	VDIN3	I	Video data input 3	
79	$\overline{\text{RE}}$	O	Read enable output	Control the read operation of field memory
80	$\overline{\text{RRST}}$	O	Read reset output	Outputs signal for initializing the read address of field memory

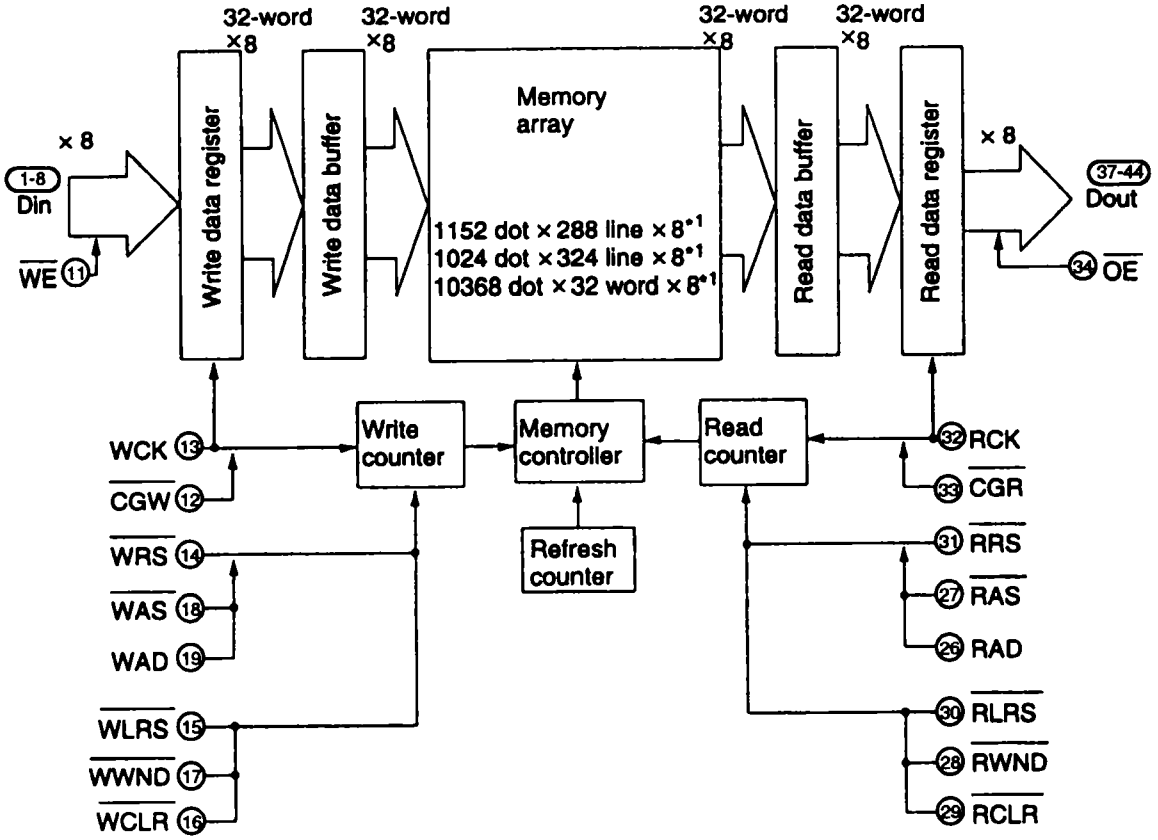
■HM530281RTT-25 (DMYC ASSY : IC102)

- 331776-word × 8bit FRAME MEMORY

•Pin Assignment (Top View)


Dout0 Dout1 Dout2 Dout3 Dout4 Dout5 Dout6 Dout7 Vss Vcc OE CGR RCK RRS RLRS RCLR RWND RAS RAD TEST1 TEST2 TEST3
44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23
(Top View)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
Din0 Din1 Din2 Din3 Din4 Din5 Din6 Din7 Vss Vcc WE CGW WCK WRS WLRS WCLR WWND WAS WAD MODE0 MODE1 TEST0

•Block Diagram



Note : 1. Selected by the mode pin

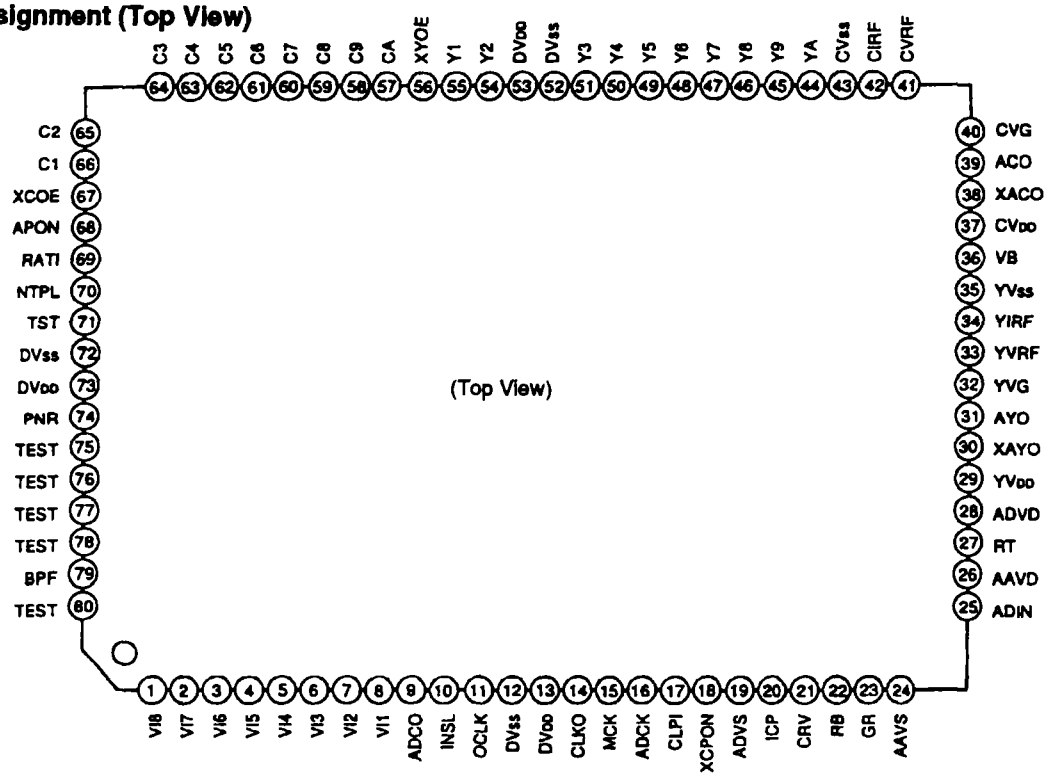
•Pin Function

No.	Pin Name	I/O	Function
1	DIN0	I	8 bit data input
2	DIN1		
3	DIN2		
4	DIN3		
5	DIN4		
6	DIN5		
7	DIN6		
8	DIN7		
9	VSS	—	Ground pin
10	VCC	—	Power supply pin
11	$\overline{WE}$	I	Signal input pin for controlling the enable/disable of data input pin
12	$\overline{CGW}$	I	Clock gate for write. Signal input pin for controlling the enable/disable the inclement of internal write address pointer.
13	WCK	I	Write clock input . Input the write data by synchronizing this clock.
14	$\overline{WRS}$	I	Write address pointer reset input. This reset input is detected the falling edge only, then it becomes write cycle of designated address by first WCK cycle after the falling edge.
15	$\overline{WLRS}$	I	Write line reset input. Signal input for reset the write address pointer from the free dot of each line to the lead.
16	$\overline{WCLR}$	I	Write clear input. Signal input for reset the write address pointer to "0" and cancel the window scan function which is irrelevant to the level of other input pin.
17	$\overline{WWND}$	I	Write window scan input. Signal input for setting the window scan function.
18	$\overline{WAS}$	I	Write address set and jump input. This input signal is detected the falling edge.
19	WAD	I	Write jump address input
20	MODE0	I	Mode selection input
21	MODE1		
22	TEST0	—	Connect to GND
23	TEST1		
24	TEST2		
25	TEST3		
26	RAD	I	Read jump address input
27	$\overline{RAS}$	I	Read address set and jump input. This input signal is detected the falling edge.
28	$\overline{RWND}$	I	Read window scan input. Signal input for setting the window scan function.
29	$\overline{RCLR}$	I	Read mode clear input. Signal input for reset the read address pointer to "0" and cancel the window scan function which is irrelevant to the level of other input pin.
30	$\overline{RLRS}$	I	Read line reset input. Signal input for reset the read address pointer from the free dot of each line to the lead.
31	$\overline{RRS}$	I	Read address pointer reset input. This reset input is detected the falling edge only, then it becomes read cycle of designated address by first RCK cycle after the falling edge.
32	RCK	I	Read clock input
33	$\overline{CGR}$	I	Clock gate for read input. Signal input pin for controlling the enable/disable the inclement of internal read address pointer.
34	$\overline{OE}$	I	Output enable input. Signal input for controlling the enable/disable of data output pin.
35	VCC	—	Power supply pin
36	VSS	—	Ground pin
37	DOUT7	O	8 bit data output
38	DOUT6		
39	DOUT5		
40	DOUT4		
41	DOUT3		
42	DOUT2		
43	DOUT1		
44	DOUT0		

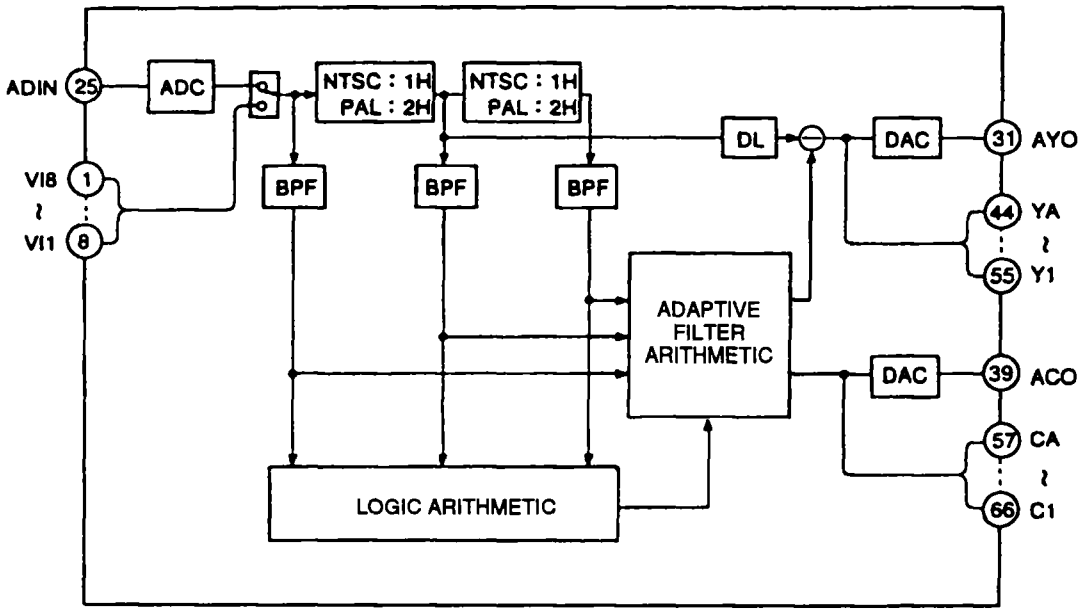
■CXD2024AQ (DMYC ASSY : IC201)

- DIGITAL COMB FILTER (NTSC/PAL)

•Pin Assignment (Top View)



•Block Diagram



•Pin Function

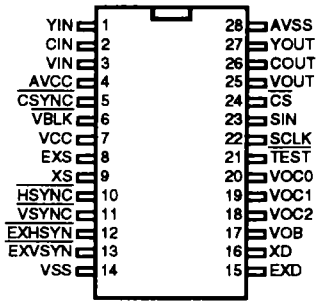
No.	Pin Name	I/O	Function
1	VI8	I	Digital input (MSB). Connect to DVDD or DVSS at not used.
2	VI7		Digital input Connect to DVDD or DVSS at not used.
3	VI6		
4	VI5		
5	VI4		
6	VI3		
7	VI2		
8	VI1		Digital input (LSB). Connect to DVDD or DVSS at not used.
9	ADCO	I	A/D converter output through mode. H : Output the video signal input from A/D converter (ADIN : pin 25) as the 8 bit digital data from Y output pins (YA : pin 44) — (Y3 : pin 51) with delayed 3.5clocks. L : Normal mode
10	INSL	I	Input switch. Switch the input data of comb filter. H : Digital input, L : Analog input
11	OCLK	I	Clock amp input. Input by DC cut with the capacitor more than 0.8Vp-p.
12	DVSS	—	Digital ground
13	DVDD	—	Digital power supply (+5V)
14	CLKO	O	Clock amp output
15	MCK	I	Master clock input. Input 4fsc clock which is locked the color burst. Normally, connect the clock amp output (CLKO : pin 14)
16	ADCK	I	Clock input for A/D converter. Input same clock as the master clock (MCK : pin 15). Normally, connect the clock amp output (CLKO : pin 14)
17	CLPI	I	Clamp pulse input for A/D converter. Clamp the signal voltage of the low period of clamp pulse. When clamp function is "OFF", connect to digital power supply (DVDD).
18	XCPON	I	Clamp setting for A/D converter. H : Clamp function turn to "OFF", then it becomes normally A/D converter function only. L : Clamp function works.
19	ADVS	—	Digital ground for A/D converter
20	ICP	I	Voltage integrated pin for clamp control. Connect a 0.01 μF capacitor. When clamp is not used, connect to analog ground (ADVS).
21	CRV	I	Clamp reference voltage input. Operate the input voltage between the reference voltage and clamp period becomes equal. When clamp is not used, connect to analog ground (ADVS).
22	RB	O	Standard value (+5V) of reference voltage (Bottom)
23	GR	—	Guard ring Connect to analog ground (AAVS).
24	AAVS	—	Analog ground for A/D converter
25	ADIN	I	Comb filter analog input (A/D converter input)
26	AAVD	—	Analog power supply (+5V) for A/D converter
27	RT	O	Standard value (+2.6V) of reference voltage (Top)
28	ADVD	—	Digital power supply (+5V) for A/D converter
29	YVDD	—	Analog power supply (+5V) for Y system D/A converter
30	XAYO	I	AYO inversion current output Connect to analog ground (YVSS).
31	AYO	O	Analog luminance signal output. Output is able to produce by connecting a resistor.
32	YVG	O	Connect a 0.1 μF capacitor
33	YVRF	I	Set the full scale value of analog luminance signal
34	YIRF	O	Connect the "16R" (16 times) resistor against to output resistor "R" of AYO pin.
35	YVSS	—	Analog ground for D/A converter of Y system
36	VB	O	Connect a 0.1 μF capacitor
37	CVDD	—	Analog power supply (+5V) for D/A converter of C system
38	XACO	O	ACO inversion current output. Connect to analog ground (CVSS).
39	ACO	O	Analog chroma signal output. Output is able to produce by connecting a resistor.
40	CVG	O	Connect a 0.1 μF capacitor

No.	Pin Name	I/O	Function
41	CVRF	I	Set the full scale value of analog chroma signal.
42	CIRF	O	Connect a "16R" (16-times) resistor against to output resistor "R" of ACO pin.
43	CVSS	–	Analog ground for D/A converter of C system
44	YA	O	Digital luminance signal output
45	Y9		
46	Y8		
47	Y7		
48	Y6		
49	Y5		
50	Y4		
51	Y3		
52	DVSS	–	Digital ground
53	DVDD	–	Digital power supply (+5V)
54	Y2	O	Digital luminance signal output
55	Y1	O	Digital luminance signal output (LSB)
56	XYOE	I	Digital luminance signal output control. H : Hi-inpedance, L : Standard output
57	CA	O	Digital chroma signal output (MSB)
58	C9		Digital chroma signal output
59	C8		
60	C7		
61	C6		
62	C5		
63	C4		
64	C3		
65	C2		
66	C1		Digital chroma signal output (LSB)
67	XCOE	I	Digital chroma signal output control. H : Hi-inpedance, L : Standard output
68	APCN	I	Aperture correction. H : Correct the frequency characteristic which is inferiored by the aperture effect. Through mode (TST : ON) also have effect on the aperture correction to Y output. L : Standard mode
69	RATI	I	Ratio setting. H : PAL PNR : At ON, forced fix to low on the inside. L : NTSC
70	NTPL	I	NTSC/PAL mode setting. H : PAL, L : NTSC
71	TST	I	Y output through mode. H:Outputs the input composite video signal from Y output. At this time, 1H (at NTSC, 2H at PAL) +18 clocks is delayed to the input (at digital input). C output is output the chroma signal which is Y/C separated. L : Y/C separation mode
72	DVSS	–	Digital ground
73	DVDD	–	Digital power supply (+5V)
74	PNR	I	PAL H : Dot interface (little) L : Dot interface (before improvement) NTSC : Fixed low
75	TEST	I	Test pin Normally, fix to low
76			
77			
78			
79	BPF	I	Y/C separation treatment mode setting. H : Fix to BPF separation mode L : Adaptation treatment mode
80	TEST	I	Test pin. Normally, fix to low

■MB90075PF-003 (DMYC ASSY : IC211)

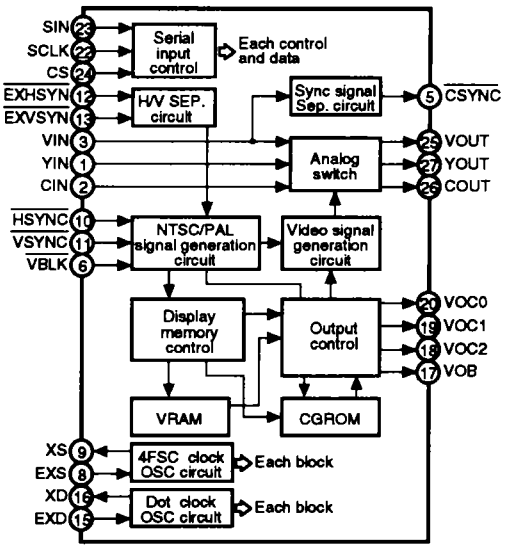
• ON SCREEN DISPLAY CONTROLLER

•Pin Assignment (Top View)



(Top View)

•Block Diagram



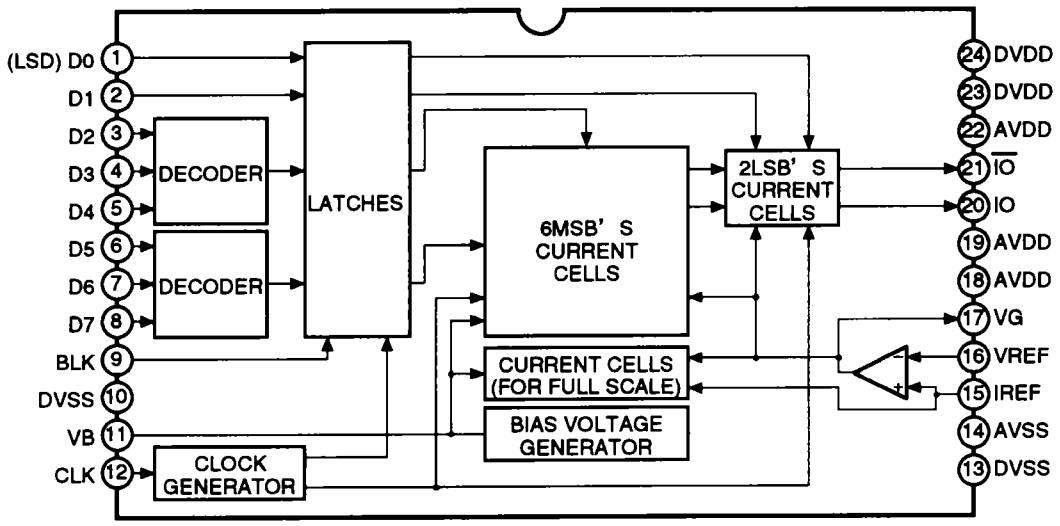
•Pin Function

No.	Pin Name	I/O	Function
1	YIN	I	Luminance signal input at superinpose display. Inputs 2Vp-p (Sync chip level :1V, pedestal level :1.57V) signal which is DC regenerated (DC clamp).
2	CIN	I	Color signal input at superimpose display. Inputs a signal of DC voltage 1.57V and amplituede of color burst signal 0.57Vp-p.
3	VIN	I	Composite video signal input at superimpose display. Input 2Vp-p (Sync chip level :1V, pedestal level : 1.57V) signal which is DC regenerated (DC clamp).
4	AVCC	–	Analog power supply. Set to same voltage as VCC.
5	$\overline{\text{CSYNC}}$	O	Composite sync signal output. Separation and detect the composite video signal input to VIN pin, then output it.
6	$\overline{\text{VBLK}}$	O	Vertical blanking period signal output. Outputs low level for a vertical blanking period.
7	VCC	–	Power supply pin
8	EXS	I	Connect the external circuit of clock generator for color burst. Crystal oscillation circuit is composed of crystal (NTSC :14.31818MHz, PAL : 17.734475MHz) and capacitor.
9	XS	O	
10	$\overline{\text{HSYNC}}$	O	Horizontal sync signal output. Use as composite sync signal output pin. Set the TEST pin to low level, outputs 4fsc clock which dividing the oscillation clock (fsc) for color burst by 4.
11	$\overline{\text{VSYNC}}$	O	Vertical sync signal output. Outputs oscillation clock for dot clock by set the TEST pin to low level.
12	$\overline{\text{EXHSYN}}$	I	External horizontal sync signal input. Use as the composite sync signal input pin. Hysteresis input with the internal pull-up.
13	$\overline{\text{EXVSYN}}$	I	External vertical sync signal input. Hysteresis input with the internal pull-up.
14	VSS	–	Ground pin
15	EXD	I	Connect the external circuit of dot clock generator for display LC oscillation circuit is composed of L and C.
16	XD	O	
17	VOB	O	Character and character back period signal output
18	VOC2	O	Character signal output. Output character color, character back color and under color.
19	VOC1		
20	VOC0		
21	$\overline{\text{TEST}}$	I	Test signal input. Normally, input high level (fixed).
22	SCLK	I	Shift clock input for serial transfer. Hysteresis input with the internal pull-up.
23	SIN	I	Serial data input. Hysteresis input with the internal pull-up.
24	$\overline{\text{CS}}$	I	Chip select input. When performing the serial transfer, set to low level. Use as release the power on reset. Hysteresis input with the internal pull-up.
25	VOUT	O	Composite video signal output. Outputs a 2Vp-p (Sync chip level :1V, pedestal level : 1.57V) signal.
26	COUT	O	Color signal output. Outputs a signal of DC voltage 1.57V and amplitude of color burst signal 0.57Vp-p.
27	YOUT	O	Luminance signal output. Outputs a 2Vp-p (Sync chip level : 1V, pedestal level : 1.57V) signal.
28	AVSS	–	Analog ground pin. Set to same voltage as VSS.

■CXD1171M (DMYC ASSY : IC301)

- 8 BIT 40MSPS D/A CONVERTER

•Block Diagram



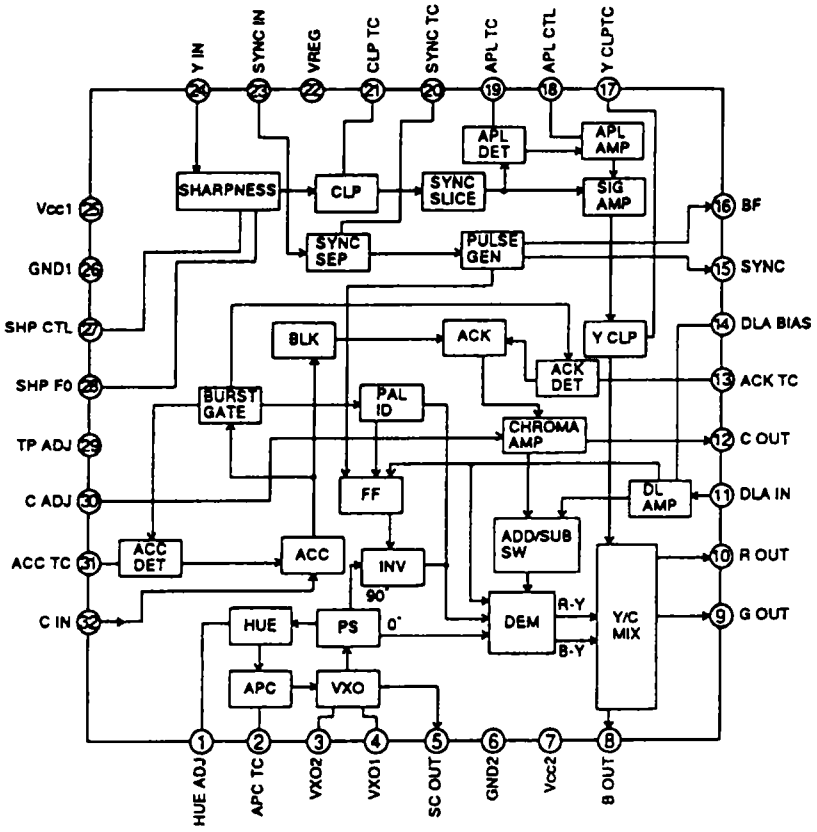
•Pin Function

No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function
1	D0	I	Digital input	13	DVSS	–	Digital GND
2	D1			14	AVSS	–	Analog GND
3	D2			15	IREF	I	Connect a "16R" (16-times) resistor against to output resistor "R".
4	D3			16	VREF	I	Set the output full scale value.
5	D4			17	VG	O	Connect the about 0.1 μF capacitor.
6	D5			18	AVDD	–	Analog VDD
7	D6			19			
8	D7			20	IO	O	Current output
9	BLK	I/O	Blanking pin H :No signal (Output 0V) L : Output state	21	$\overline{IO}$	O	Inversion current output. Normally, connect to analog GND.
10	DVSS	–	Digital GND	22	AVDD	–	Analog VDD
11	VB	I	Connect the about 0.1 μF capacitor.	23	DVDD	–	Digital VDD
12	CLK	I	Clock input	24			

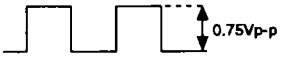
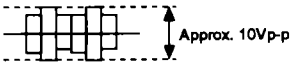
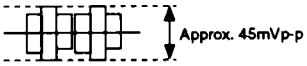
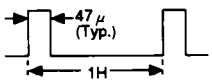
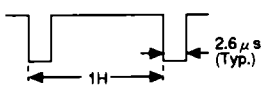
■CXA1585Q (DMYC ASSY : IC701)

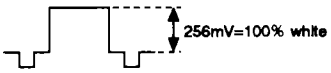
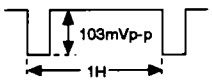
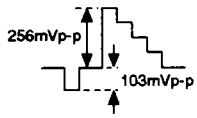
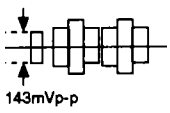
• R. G. B. DECODER

•Block Diagram



•Pin Function

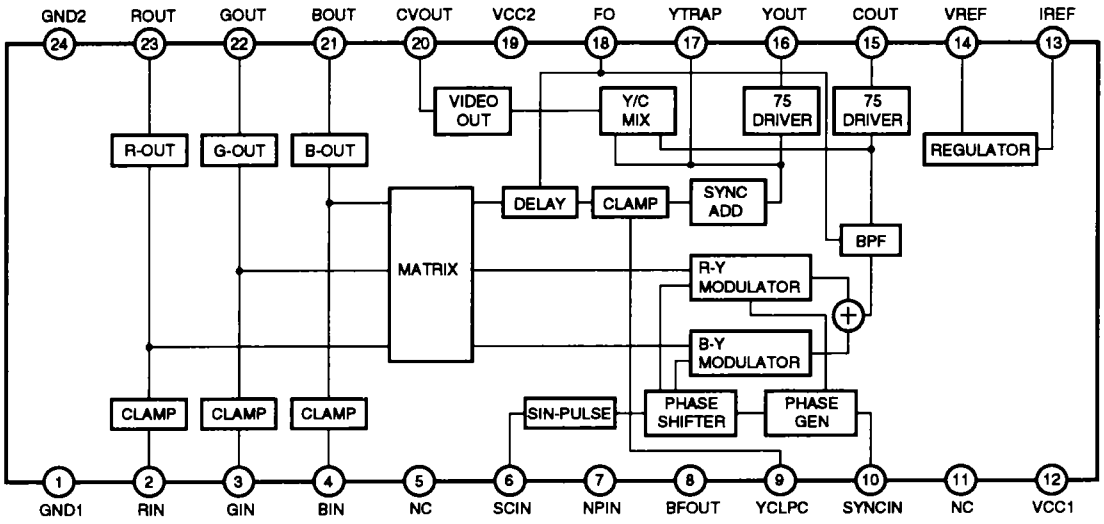
No.	Pin Name	Function
1	HAU ADJ	HAU adjustment pin
2	APCTC	APC (color sync) time constant and free-run frequency adjustment pin
3	VXO2	Crystal oscillator pin
4	VXO1	
5	SC OUT	Subcarrier output pin
6	GND2	Chroma system GND pin
7	VCC2	Chroma system VCC pin
8	B OUT	B output pin * at 75% color-bar reference level input
9	G OUT	G output pin
10	R OUT	R output pin 
11	DLA IN	Dlay line amp input pin. At NTSC mode, connect to GND. At PAL mode, connect to 1H delay line input. 
12	C OUT	Chroma output pin at PAL. At NTSC mode, connect to VCC. At PAL mode, connect to 1H delay line input. 
13	ACK TC	ACK (Auto Color Killer) time constant pin
14	DLA BIAS	NTSC/PAL mode switch and delay line amp gain adjustment pin. NTSC mode : V14≦0.8V PAL mode : 2.0V≦V14≦2.6V Variable range : Mode than ±2db
15	SYNC	Composite sync output pin. Outputs active high 
16	BF	Burst flag output pin. Outputs active low 

No.	Pin Name	Function
17	Y CLP TC	Pedestal clamp time constant pin
18	APL CTL	APL sensitivity adjustment pin. Control limit is 3-5V. If APC control is not performed, connect to GND.
19	APL TC	Time constant pin for detecting the APC (Average Picture Level) of luminance signal. APL 0% V19 = 2.0V (Typ.) APL 100% V19 = 3.2V (Typ.) 
20	SYNC TC	Sync chip clamp time constsnt pin for SYNC SEP
21	CLP TC	Pedestal clamp time constant pin
22	VREG	4.2V regurator output pin with decoupling capacitor. Not used for the external power supply.
23	SYNC IN	Signal input pin for SYNC SEP. Standard SYNC level is 103mVp-p. Normally, short-circuit between this pin and YIN (pin 24). 
24	Y IN	Y signal input pin ・Standard input level SYNC :103mVp-p 100% white : 256mVp-p Excepting the burst signal 
25	VCC1	Y system VCC pin
26	GND1	Y system GND pin
27	SHP CTL	Sharpness gain adjustment pin Variable range -4.5dB — +4.5dB (1.5V ≦ V27 ≦ 3.5V)
28	SHP F0	Filter frequency adjustment pin for sharpness
29	TP ADJ	Pulse timing setting pin for using the internal IC Connect a 2.7kΩ resistor between this pin and GND.
30	C ADJ	Chroma amp gain adjustment pin Variable range -20 — +8dB (1.5V — 3V)
31	ACC TC	ACC (Auto Color Adjustment) time constant pin
32	C IN	Chroma signal input pin. Standard input level is the burst amplitude 143mVp-p. 

■CXA1645M (DMYC ASSY : IC702)

• RGB ENCODER

•Block Diagram



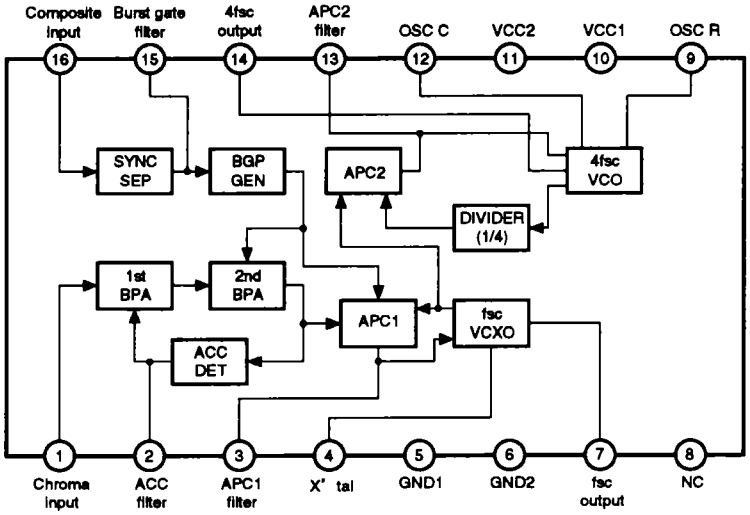
•Pin Function

No.	Pin Name	I/O	Function
1	GND1	–	Ground pin except for RGB outputs, composite video output and Y/C output circuits.
2	RIN	I	Analog RGB signal input pin.
3	GIN		
4	BIN		
5	NC	–	No connection.
6	SCIN	I	Subcarrier input pin.
7	NPIN	I	NTSC, PAL mode switching pin. NTSC: VCC PAL: GND
8	BFOUT	O	Output pin for monitoring the BF pulse. 75Ω load is not able to drive.
9	YCLPC	I	Y signal clamp time constant pin. Connect a capacitor (0.1 μF) to ground.
10	SYNCIN	I	Composite sync. signal input pin. Input by TTL level. At L (≦0.8V) , H (≧2.0V) : SYNC period
11	NC	–	No connection.
12	VCC1	–	Power supply pin except for RGB outputs, composite video output and Y/C output circuits.
13	IREF	O	Settle pin for internal reference current. Connect a resistor (47kΩ) to ground.
14	VREF	O	Internal reference voltage pin. Perform to decup with a capacitor (approx. 10 μF).
15	COUT	O	Chroma signal output pin. 75Ω load is able to drive.
16	YOUT	O	Y signal output pin. 75Ω load is able to drive.
17	YTRAP	I	Eliminating the cross color of subcarrier frequency element which is included in Y signal.
18	FO	O	fo adjustment pin of internal filter. Connect a following resistor in accordance with NTSC/PAL mode to ground. NTSC : 20kΩ (±1%) PAL : 16kΩ (±1%)
19	VCC2	–	Power supply pin of RGB outputs, composite video output and Y/C output circuits. Perform to decup with a capacitor (more than 10 μF) because of the large current is flowed.
20	CVOUT	O	Composite video signal output pin. 75Ω load is able to drive.
21	BOUT	O	Analog RGB signal output pin. 75Ω load is able to drive.
22	GOUT		
23	ROUT		
24	GND2	–	Ground pin of RGB outputs, composite video output and Y/C output circuits.

■MM1093PF (DMYC ASSY : IC401)

• 4fsc CLOCK GENERATOR

•Block Diagram

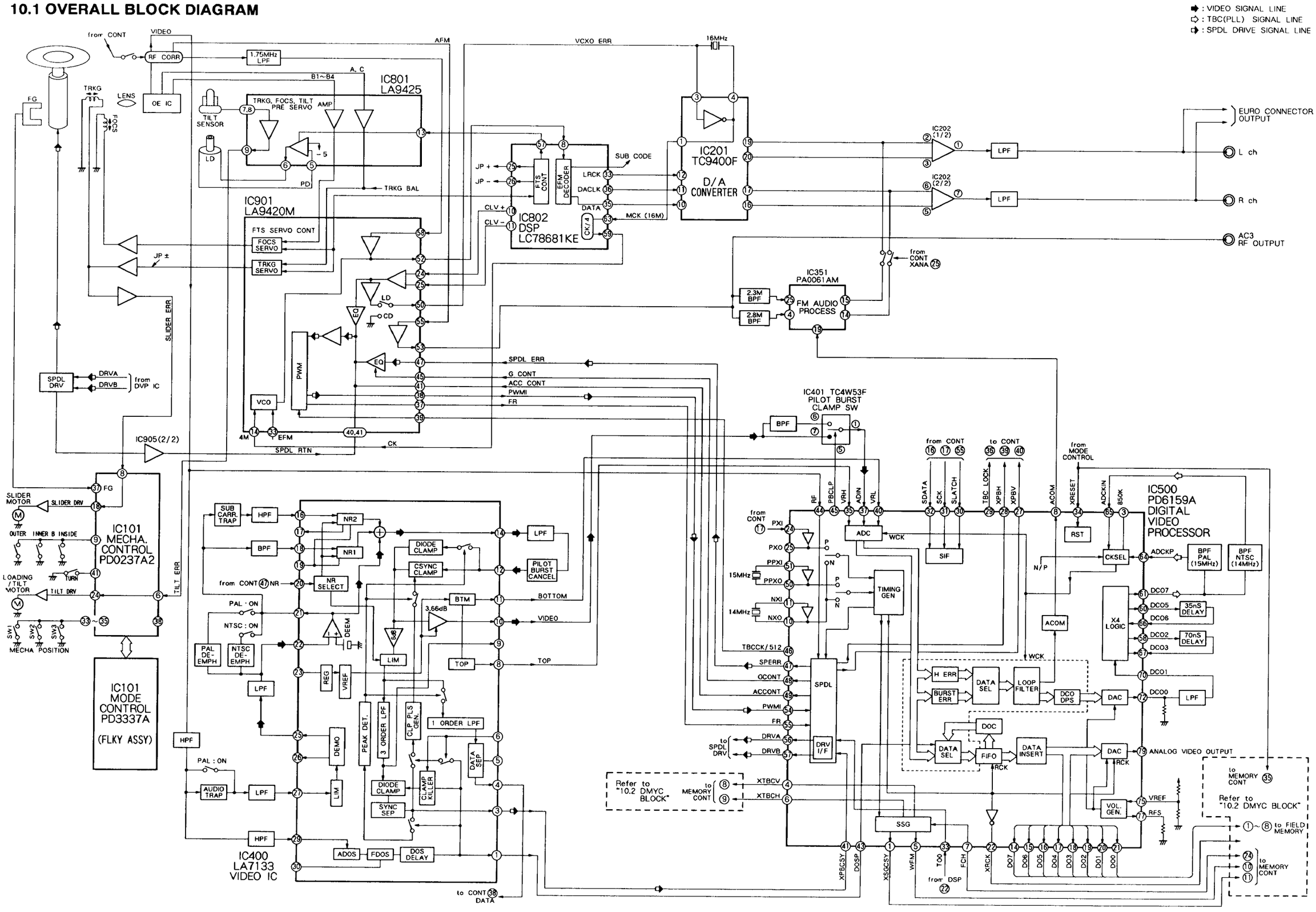


•Pin Function

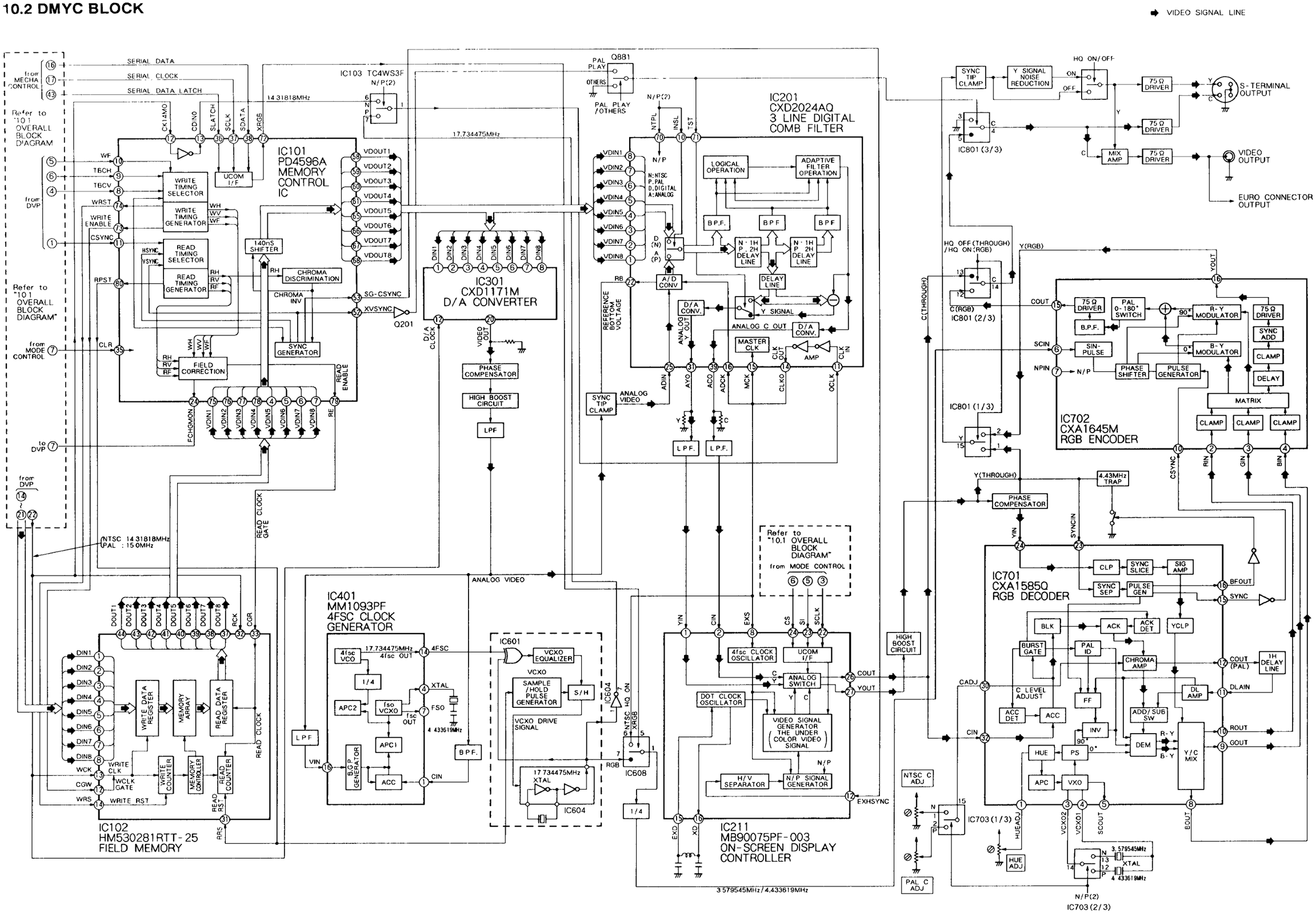
No.	Pin Name	Function
1	Chroma input	Chroma signal input pin
2	ACC filter	ACC filter pin
3	ACC1 filter	Filter pin of fsc system APC circuit
4	X' tal	X' tal pin of VCXO circuit
5	GND1	fsc system GND pin
6	GND2	4fsc system GND pin
7	fsc output	Outputs a subcarrier which synchronizing the input chroma signal
8	NC	Non connection
9	OSC R	Connect a resistor which deciding the free-run frequency of 4fsc VCO
10	VCC1	fsc system power supply pin
11	VCC2	4fsc system power supply pin
12	OSC C	Connect a capacitor which deciding the free-run frequency of 4fsc VCO
13	APC 2 filter	Filter pin of 4fsc system APC circuit
14	4fsc output	Outputs a signal multiplied by 4 with synchronizing the input chroma signal.
15	Burst gate filter	Burst gate filter pin
16	Composite input	Composite signal input pin

10. BLOCK DIAGRAMS

10.1 OVERALL BLOCK DIAGRAM



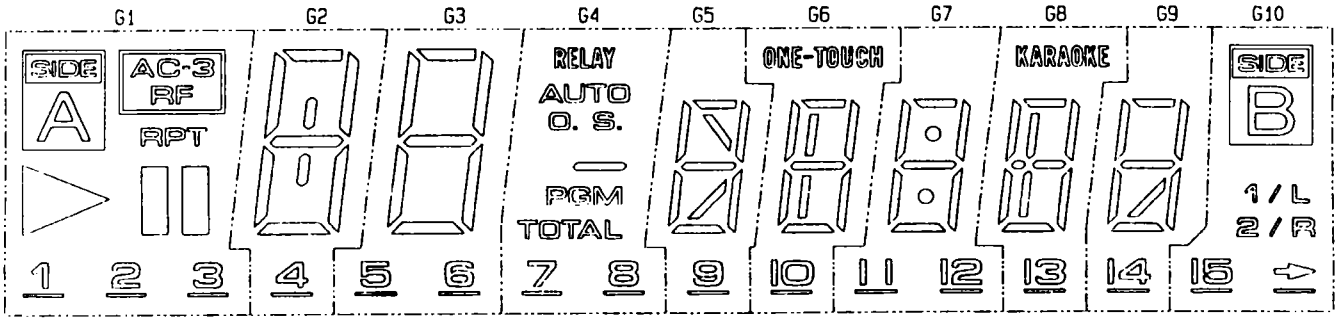
10.2 DMYC BLOCK

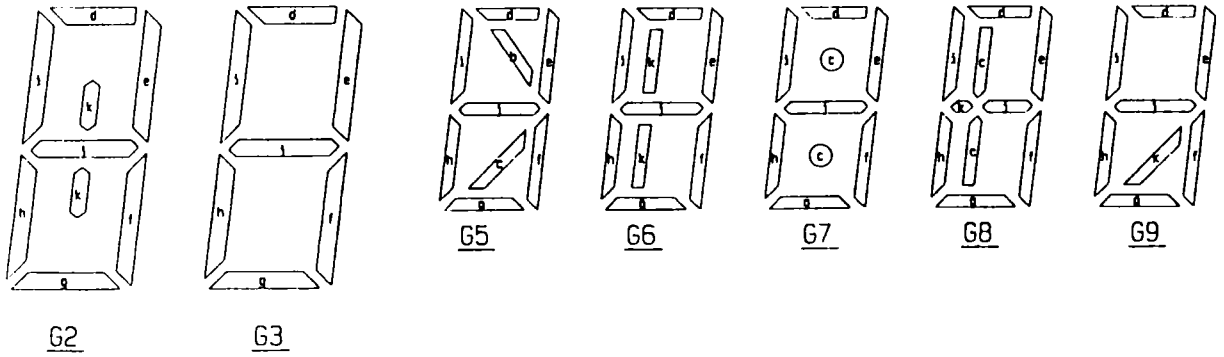


11. FL INFORMATION

■ VAW1041 (FLKY ASSY : V101)

• FL TUBE





• ANODE GRID ASSIGNMENT & PIN ASSIGNMENT

	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
P1	1	4	5	7	9	10	11	13	14	15
P2	2		6	8	b	ONE-TOUCH	12	KARAOKE		
P3	3				c			c		
P4	SIDE A	d	d	RELAY	d	d	d	d	d	SIDE B
P5	▷	e	e	AUTO	e	e	e	e	e	1/L
P6	▯▯	f	f	O.	f	f	f	f	f	2/R
P7	RPT	g	g	S.	g	g	g	g	g	
P8	AC-3 RF	h	h	-	h	h	h	h	h	
P9		i	i	PGM	i	i	i	i	i	
P10		j	j	TOTAL	j	j	j	j	j	
P11		k				k		k	k	

• PIN ASSIGNMENT

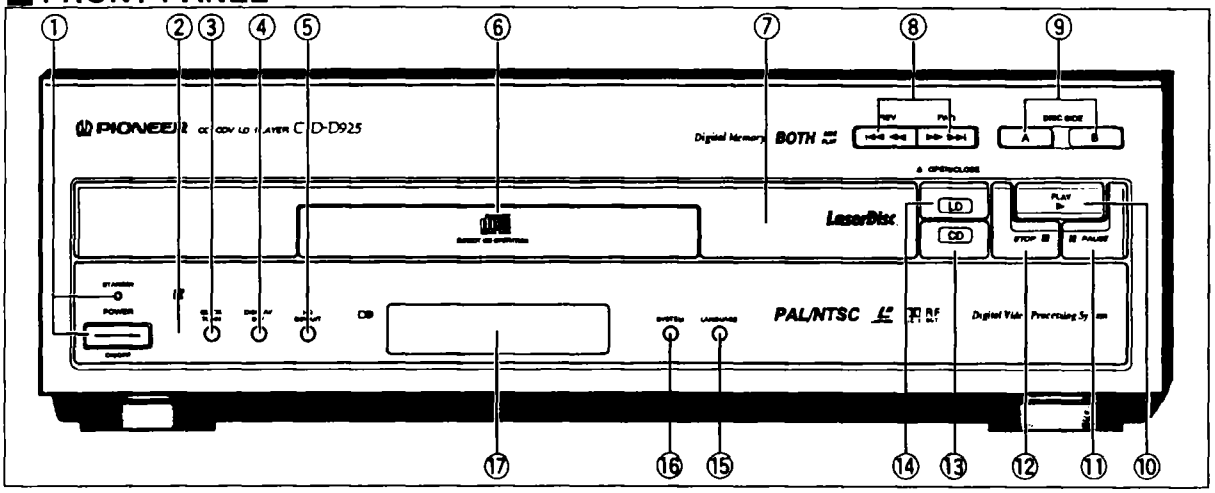
Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Assignment	F	F	NP	NL	NL	NL	NL	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10

Pin No.	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
Assignment	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	NL	NL	NL	NP	F	F

F:Filament G1~G10:Grid P1~P11:Anode NP:No pin NL:No Lead

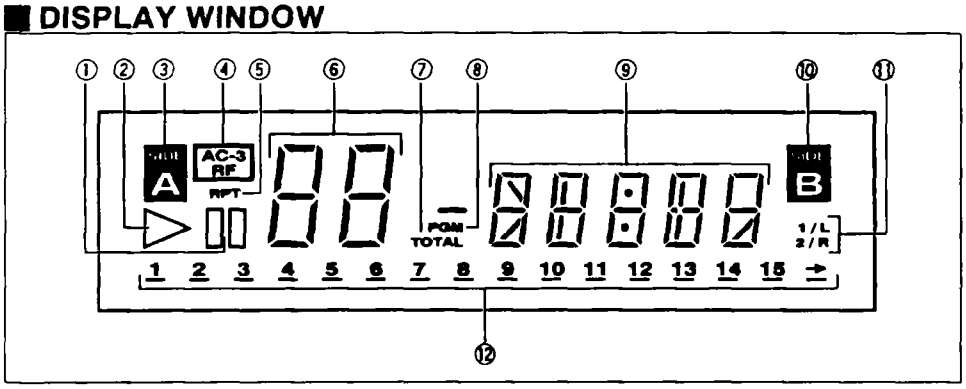
12. PANEL FACILITIES

■ FRONT PANEL



① **POWER ON/OFF switch and STANDBY indicator**
Press to turn the power on and off.
② **Remote sensor**
③ **QUICK TURN button/indicator**
④ **DISPLAY OFF button/indicator**
⑤ **HQ CIRCUIT button/indicator**
⑥ **CD disc table**
⑦ **Disc table**
⑧ **Track/manual search (|◄◄ ◄◄, ►► ►►|) buttons**
⑨ **DISC SIDE A/B buttons/indicator**
⑩ **PLAY button (►)**
⑪ **PAUSE button (II)**
⑫ **STOP button (■)**
⑬ **CD OPEN/CLOSE (≜) button/indicator**
⑭ **LD OPEN/CLOSE (≜) button/indicator**
⑮ **LANGUAGE button**
⑯ **SYSTEM button**
⑰ **Display window**

■ DISPLAY WINDOW



① **II pause indicator**
Lights when the player is in pause mode.
② **► play indicator**
Lights during play. Blinks during search.
③ **DISC SIDE A indicator**
④ **AC-3 RF indicator**
Lights when a DOLBY SURROUND AC-3 disc is being played back.
⑤ **RPT (repeat) indicator**
Lights during repeat play.
⑥ **Track/chapter indicator**
Indicates the track number or chapter number.
⑦ **TOTAL indicator**
Indicates the TOTAL TIME (total play time).
⑧ **PGM (program) indicator**
Lights during program play.
⑨ **Time/mode indicator**
Indicates the elapsed playing time, remaining playing time, total time or mode.
⑩ **DISC SIDE B indicator**
⑪ **1/L, 2/R indicator**
Indicates the audio output channel.
⑫ **LD/CD/CDV visual calendar**
When a disc is loaded, all of the chapter/track numbers recorded on the disc light up on the display. If the disc contains more than 15 chapters/tracks, the → indicator lights.
During program play, only the programmed chapter/track numbers light. When a disc without a TOC section is played, only the selection number being played lights.
When a CDV disc is loaded, the track numbers of the video part light followed by the track numbers of the audio part. After a chapter/track is finished playing, the corresponding number goes out.

13. SPECIFICATIONS

1. General

System ..... LaserVision Disc system and Compact Disc digital audio system
Laser ..... Semiconductor laser wavelength 780 nm
Power requirements ..... AC 220 ~ 240 V, 50/60 Hz
Power consumption ..... 51 W
Weight ..... 6.8 kg
Dimensions ..... 420 (W) x 407 (D) x 132 (H) mm
Operating temperature ..... +5°C ~ +35°C
Operating humidity ..... 5% ~ 85%
(There should be no condensation of moisture.)

2. Video characteristics

Format ..... PAL/NTSC specifications
Video output
- Level ..... 1 Vp-p nominal, sync. negative, terminated
- Impedance ..... 75Ω unbalanced
- Jack ..... RCA jack

S-Video output
- Y (luminance) level ..... 1 Vp-p (75Ω)
- C (color) level ..... 286 mVp-p (75Ω)
- Jack ..... S-VIDEO jack

3. Audio characteristics

Output level
- During analog audio output ..... 200 mVrms (1 kHz, 40%)
- During digital audio output ..... 200 mVrms (1 kHz, –20 dB)

Jacks ..... Both RCA jacks
Number of channels 2

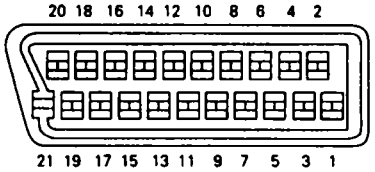
Digital Audio Characteristics

Frequency response	4 Hz - 20 kHz
SN ratio	115 dB (EIAJ)
Dynamic range	97 dB (EIAJ)
Total harmonic distortion	0.003 % (EIAJ)
Wow and flutter	Limit of measurement (EIAJ)

4. Other Terminals

Control input/output ..... Both miniature jacks
Optical digital output ..... Optical digital jack
AC-3-RF output ..... RCA jack
AV connector input/output ..... 21-pin connector
This connector provides the video and audio signals for connection to a colour video TV monitor (or TV set) which has a "AV CONNECTOR" terminal.

PIN assignment



PIN no.		
1	Audio 2/R out	17 GND
3	Audio 1/L out	19 Video out
4	GND	21 GND
8	Status	

5. Accessories

Remote control unit 1
Size "AAA" (IEC R03) dry cell batteries 2
Euroconnector cable 1
Power cord 1
Audio cord 1
Operating instructions 1
Warranty card 1

NOTE:
The specifications and design of this product are subject to change without notice, due to improvements.